

# THE COMPUTER JOURNAL<sup>®</sup>

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# Editor's Page

## Formulating Our Product Review Policy

Recently we received a letter that said:

"I don't think you should do reviews for new products. This is what has hurt all the other magazines—their need to be current, trendy, with-it. *The Computer Journal* should be behind the times by supporting the end user after he or she has bought their system and then says "What Now?"

It was a thought-provoking letter with some good points, and it made the staff here at *The Computer Journal* think a lot about our then-unstated product review policy.

We feel that one of the purposes of a journal is to bring information on new product developments to the attention of the readers, but it is true that some magazines have reached the point where new product releases and product reviews take up the majority of the space.

There is a difference between a product announcement, which is usually written from the vendor's literature, and a product review, which requires working with the product in an actual application long enough to find out how it really performs. A so-called "review" written from the manual with a quick run on the computer is useless.

Our product information should follow in the same vein as the majority of our articles by providing specific technical information that will be of use to those who "build, interface, and apply micros." As a general rule, if it is covered in *Byte* and *InfoWorld*, we do not need to rehash the same information by covering it in *The Computer Journal*.

The areas we intend to cover in our product reviews are utilities, languages, sensors, boards, interfaces, peripherals, etc. We may occasionally report on products which have been covered elsewhere, but we will concentrate on the technical aspects of the products and not just repeat what you have already read.

A good review involves a lot of work, and we don't have the time to spend on products which do not interest our readers. We would appreciate your feedback on the subject of product reviews. Some of

the products we have for review are: Conix (a CP enhancement), ACNAP (an AC circuit analysis program), PLOTPRO (a plotting program which works with ACNAP), SPP (a signal processing program), FORTH-83, and Condor-3.

Tell us which ones we should eliminate, and suggest items that you think we should add to our list. We would also like to incorporate your experience with the product into the reviews, or use them as added comments in a future issue.

Our policy henceforth will be to review technical products which are of interest to our readers, but to avoid reviewing systems and general interest items which are covered in other publications. We don't want to use an excessive amount of space for new product announcements and product reviews, but since other publications are not presenting the detailed technical reviews our readers demand, we will concentrate on presenting needed information. ■

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# READING PC DOS DISKETTES WITH THE MORROW MICRO DECISION

by Lance Rose, Technical Editor

With all the different 5¼ inch diskette formats around today, it's not surprising that there is little compatibility from one manufacturer's equipment to another, even within the realm of CP/M systems. Add to this the fact that aside from CP/M systems there is the IBM PC and its lookalikes with their own operating system known as PC DOS, and you have a real mess.

Here at *The Computer Journal* we are constantly faced with the problem of potential articles being submitted on a variety of diskette formats and not always having the right machine around to read them on. Fortunately, we do have an 8-inch CP/M system and an Apple which helps quite a bit. Nevertheless, until recently we have been dependent on other facilities to read any diskette that came in written on a PC.

Recently we acquired a Morrow Micro Decision with double-sided minifloppy drives. Morrow has thoughtfully provided several utility programs with the system that can enable the machine to read diskettes made on the Osborne, Xerox and IBM disk systems. The catch is that only the CP/M-86 format is supported for the PC. Unfortunately for us, PC DOS is the de-facto standard for the PC and almost no one uses CP/M-86 on it. The question was, how do we use this utility to read files from a PC DOS diskette?

Luckily, it turns out that PC DOS and CP/M-86 for the IBM PC both use the same type of physical diskette formatting, namely 512-byte sectors. Depending on which version of PC DOS we're talking about, there are eight (Version 1) or nine (Version 2) sectors per track. In addition, for the double-sided formats of PC DOS, the diskette is organized in cylinders. This means that track 0 side 0 is used first, then track 0 side 1, followed by track 1 side 0, etc. Fortunately, this is the same arrangement used in the Micro Decision double-sided format. By simply running the IBM.COM utility to set drive B to an IBM drive and changing a byte in the drive description table we can also read double sided PC DOS diskettes.

With the physical format compatibility problems handled by IBM.COM, we can turn our attention to the logical layout of PC DOS diskettes and how they differ from CP/M diskettes. In CP/M, each directory entry is 32 bytes long and contains the user number, file name and type, number of 128-byte records in the file, and a list of up to 8 "allocation block numbers" which point to the areas of the diskette where the file is to be found. Since in many systems these blocks are 2K bytes each, the directory entry can represent files up to 16K in size. The problem here is that if the file is over 16K bytes long, we need a second directory entry to hold the additional allocation block numbers for the file. For example, a file that was 87K long would require 6 entries

(192 bytes) in the directory to represent it.

This isn't a very efficient use of directory space and it may be one reason that Microsoft chose a different directory format for their MSDOS/PC DOS operating system. In this system, there is a file allocation table (FAT) on track 0 of each diskette. This table contains linked lists of the sectors allocated to each file. The directory, which is located on track 0 immediately following the FAT, consists of 32-byte entries, like CP/M. Each entry contains the file name and type, file size in bytes, and a pointer into the file allocation table. This pointer identifies the first sector allocated to a file. The succeeding pointers are in the FAT itself, of course. The advantage here is that only two bytes are necessary in the directory entry itself to point to the linked list as opposed to 16 bytes for each CP/M entry. There are two immediate advantages to this. First, the additional bytes in the 32-byte directory entry can be used for time and date stamping which PC DOS supports. Secondly, only one entry is required no matter how large the file.

With this in mind, and the PC DOS manual in hand, one can read the FAT and directory into memory, display the contents of the directory, and/or read a file from the diskette by following the linked list of allocated sectors using the mapping algorithm described in the PC DOS manual.

Listing 1 is an assembly listing of a program that will read a PC DOS directory and display its contents in a format similar to the CP/M DIR command. In addition, the size of each file is also displayed, rounded up to the nearest 1k bytes. This allows the user to examine the PC DOS diskette in drive B and see what files, if any, he wants to transfer to the CP/M diskette in drive A. The program is run by typing: DIRPC (return).

Listing 2 is an assembly listing of a program that searches the PC DOS directory for a given file and then, if found, copies it to the CP/M diskette in drive A. For example, if the user wants to copy a file named LETTER.TXT, he would type: READPC LETTER.TXT (return). A message is displayed if the file isn't found; otherwise the copy is made. When finished reading PC DOS diskettes, the program MORROW.COM can be run to set drive B back to a Morrow drive.

These programs will work on both the Micro Decision MD-2 (single sided drives) and MD-3 (double sided drives) as long as the PC DOS diskette is single sided. In addition, if you have an MD-3, the program will detect double-sided PC DOS diskettes and read them as well. We plan to make good use of it here at *The Computer Journal* office.

Although not our immediate goal, it would also be possible to go the other way, i.e. transfer CP/M files to a

PCDOS diskette. To do this, one would have to search the FAT for empty sectors and build the linked list as the file is transferred. Should any of our ambitious readers come up with such a program, we would very much like to hear about it. (Listings 1 and 2 follow.)

## Listing 1

```

; DIRPC.ASM
; Program to display directory and file size of an
; IBM PCDOS diskette in Drive B of a Morrow Micro
; Decision, assuming IBM.COM has already been run
; to set Drive B to an IBM type diskette
; Version of 4/24/84
ROOT EQU 0000H ;CP/M reboot address
BDOS EQU 0005H ;BDOS entry point
TBUFF EQU 0000B ;Transient disk buffer
;
; ORG 100H
;
LXI SP,STACK ;Set up local stack
LDA BOOT+2
STA SELDSK+2 ;Patch for BIOS calls
STA SETTRK+2
STA SETSEC+2
STA SETDMA+2
STA READ+2
MVI C,1
CALL SELDSK ;Select P drive
MVI C,0
CALL SETTRK ;Set track 0
MVI C,5
CALL SETSEC ;Set logical sector 5
CALL READ ;Read first part of FAT
ORA A
JNZ BOOT ;Read error
LHLD BOOT+1 ;Locate drive table (MTAB)
LXI D,41H
DAD D
MOV E,M
INX H
MOV D,M
LXI H,9
DAD D ;HL points to drive B entry
LXI D,FMTERR ;In case unreadable
LDA TBUFF ;Get first byte of FAT
LXI B,10BDH ;Sector count & first sector
INR A
JZ DOUBLE ;DOS 1.0 double sided
MVI B,10B
INR A
JZ SINGLE ;DOS 1.0 single sided
LXI B,1015B
INR A
JZ DOUBLE ;DOS 2.0 double sided
MVI B,10B
INR A
JNZ EXIT ;Not DOS 2.0 single sided
SINGLE: INX B
MOV A,M
ANI 0FH ;Set media bit to single sided
MOV M,A
JMP RDIR
DOUBLE: MOV A,M
ANI 20H ;Test double sided drive bit
JZ EXIT ;Single sided drive, no read
INX H
MOV A,M
ORI 04H ;Mark media double sided
MOV M,A
RDIR: LXI H,DIRBUF ;Point at directory buffer
RDIR1: PUSH B ;Save sector
PUSH H ;Save DMA address
CALL SETSEC
POP B
PUSH B
CALL SETDMA
CALL READ
POP H
POP B
ORA A
JNZ BOOT ;Exit if disk error
PUSH B
LXI H,-0920H
DAD B
MOV A,H
ORA L
JZ RDIR2 ;Go to next side
LXI B,-0D24H
DAD B
MOV A,H
ORA L
JNZ RDIR3 ;Stay on same side
RDIR2: PUSH B
MVI C,1 ;Go to track 1
CALL SETTRK
POP B
MVI C,0 ;Start with sector 1
RDIR3: POP B
LXI D,126
DAD D ;Go to next DMA address
INR C ;Next sector
DCR B ;Decrease sector count
JNZ RDIR1
MOV A,H ;Calculate directory size
LXI B,DIRBUF
SUB H
ADD A ;8 entries per page
ADD A
ADD A
MOV C,A ;Maximum entries in C
NEXTENT: MOV A,M
CPI ' '
JC EMPTY ;Not printing ASCII
CPI 7FH
JNC EMPTY ;Same, assume empty
PUSH B ;Save count
PUSH H ;Save pointer
MOV A,B
ANI 03H
JNZ MIDLIN
LXI D,CRLF
CALL DSPLY ;Do a CRLF at beginning
MIDLIN: MVI DSPENT ;Skip separator
CALL WRTCON ;Display separator between
CALL SPACE ;Add a space
DSPENT: POP H ;Restore entry pointer
PUSH H
MVI C,8 ;Filename characters
CALL NAME ;Display filename
CALL SPACE ;Separate with space
MVI C,3 ;Display filetype
CALL NAME ;Display filetype
CALL SPACE ;Trailing space
LXI D,17
DAD D ;Point at file size
MOV E,M ;Get size in registers
INX H
MOV D,M
INX H
MOV A,M
LXI H,3FFH ;Round up to nearest 1k
DAD D
ACI 0
MOV L,H ;Shift right 10 bits
MOV H,A
MVI C,2
SHIPTR: XRA A
MOV A,H
RAR
MOV H,A
MOV A,L
RAR
MOV L,A
DCR C
JNZ SHIPTR
XRA A
STA NONZRO ;Non-zero flag
LXI D,-100
CALL DIGIT ;Display hundreds
LXI D,-10
CALL DIGIT ;Display tens
MOV A,L
ADI '0'
MOV E,A
CALL WRTCON ;Display ones
MVI E,'k' ;Add 'k' to size
CALL WRTCON ;Add a trailing space
POP B
POP B
EMPTY: LXI D,32
DAD D ;Go to next entry
DCR C
JNZ NEXTENT ;More entries to check
MOV A,B
ORA A
LXI D,NOFILE
JZ EXIT ;No entries
LXI D,CRLF ;At least one entry
CALL DSPLY ;Display message
JMP BOOT ;Reboot
DSPLY: MVI C,9 ;Display string function
JMP BDOS
SPACE: MVI E,' ' ;Display space
WRTCON: PUSH B ;Write console function
PUSH H
MVI C,2
CALL BDOS
POP H
POP B
RET
NAME: MOV E,M
CALL WRTCON
INX H
DCR C
JNZ NAME
RET
DIGIT: MVI A,'0'-1 ;Initialize digit
DAD D ;Divisor in DE
INR A ;ASCII digit in A
JC DIGIT1 ;Save digit
PUSH PSW
MOV A,L ;Correct for overflow
SUB E
MOV L,A
MOV A,H
SBB D
MOV H,A
POP PSW
MOV E,A ;Digit in E
CPI '0'
JZ DIGIT2 ;Zero in this place
MVI A,0FFBH
STA NONZRO ;Set flag
JMP WRTCON
ORA A
JNZ WRTCON ;Display embedded zero
MVI WRTCON ;Suppress leading zeros
SELDK: JMP 001BH ;Values are filled in
SETTRK: JMP 001EH
SETSEC: JMP 0021H
SETDMA: JMP 0024H
READ: JMP 0027H
;
FMTERR: DB '*** UNREADABLE PCDOS FORMAT ***'
NOFILE: DB 0DH,0AH,07H,'$'
CRLF: DB 0DH,0AH,'$'
MONZRO: DS 1 ;Flag for non-zero value
DS 48 ;Stack area
STACK EQU $
;
; ORG ($+0FFB) AND 0FF00H
;
DIRBUF: DS 7*200H ;PCDOS directory
;
END

```

## Listing 2

```

READPC.ASM
;
; Program to copy a file from an IBM PC/DOS diskette
; in Drive B to a CP/M file on Drive A of a Morrow
; Micro Decision, assuming IBM.COM has already
; been run to set Drive B to an IBM type diskette
; Version of 4/24/84
;
BOOT EQU 0000H ;CP/M reboot address
BDOS EQU 0005H ;BDOS entry point
DSTFCB EQU 005CH ;Destination FCB
;
;
; ORG 100H
;
; Set up local stack
LXI SP,STACK
LDA BOOT+2
STA SELDSK+2 ;Patch for BIOS calls
STA SETTRK+2
STA SETSEC+2
STA SETDMA+2
STA READ+2
MVI C,1
CALL SELDSK ;Select B drive
MVI C,8
CALL SETTRK ;Set track B
LXI B,0405H ;Read FAT
LXI H,FAT
RDFAT: PUSH B ;Save sector
CALL SETSEC ;Save DMA address
POP B
PUSH B
CALL SETDMA
CALL READ
POP H
POP B
ORA A ;Reboot if disk error
JNZ BOOT
LXI D,120H ;Go to next DMA address
DAI D ;Next sector
INR C ;Decrease sector count
DCR B
JNZ RDFAT ;Locate drive table (MTAB)
LHLD BOOT+1
LXI D,41H
DAD D
MOV E,M
INX H
MOV D,M
LXI H,9
DAI D ;DE points to drive B entry
XCHG ;Get first byte of FAT
LDA FAT
LXI B,1C00H ;Sector count & first sector
LXI H,0600H ;CLOFF and SPT
INR A
JZ DOUBLE ;DOS 1.0 double sided
MVI B,10H
LXI H,0A:00H
INR A
JZ SINGLE ;DOS 1.0 single sided
LXI B,1C15H
LXI H,0B09H
INP A
JZ DOUBLE ;DOS 2.0 double sided
MVI B,10H
LXI H,0F12H
INR A
JZ SINGLE ;DOS 2.0 single sided
NOREAD: LXI D,FMTEER ;Unreadable
JMF EXIT
SINGLE: INX D
LDAX D ;Set media bit to single sided
ANI 0F0H
STAX D
MVI A,03H ;Mask
JMF RDDIR
DOUBLE: LDAX D
ANI 20H ;Test double sided drive bit
JZ NOREAD ;Single sided drive, no read
INX D
LDAX D ;Mark media double sided
ORI 04H
STAX D
MVI A,07H
ANI CLMASK ;Double sided mask
STA SPT ;Save format info
SHLD SPT ;Point at directory buffer
LXI H,DIRBUF
RDDIR1: PUSH B ;Save sector
PUSH H ;Save DMA address
CALL SETSEC
POP B
PUSH B
CALL SETDMA
CALL READ
POP H
POP B
ORA A ;Exit if disk error
JNZ BOOT
PUSH B
LXI H,-0920H
DAD B
MOV A,H
ORA L
JZ RDDIR2 ;Go to next side
LXI H,-0D24H
DAD B
MOV A,H
ORA L
JNZ RDDIR3 ;Stay on same side
RDDIR2: PUSH B ;Go to track 1
MVI C,1
CALL SETTRK
POP B
MVI C,0 ;Start with sector 1
RDDIR3: POP H
LXI D,120H
DAD D ;Go to next DMA address
INR C ;Next sector
DCR B ;Decrease sector count
JNZ RDDIR1
MOV A,B ;Calculate directory size
LXI B,DIRBUF
SUB H
ADD A ;8 entries per page
ADD A

```

```

ADD A ;Maximum entries in B
MOV B,A ;Point at filename
LXI D,DSTFCB+1 ;Save pointers
SEARCH: PUSH B
PUSH H ;Length of filename/type
MVI C,11
COMPAR: LDAX D
CMP M ;Not the same
JNZ DIFFER
INX D
INX H
DCR C
JNZ COMPAR
JMP FOUND ;Entry matched
DIFFER: POP B
LXI D,32
DAD D ;Go to next entry
POP D
DCR B
JNZ SEARCH ;Not found
LXI D,FMFERR
JMP EXIT
FOUND: POP D ;Balance stack
POP D ;Save pointer to entry
MVI C,8
CALL SELDSK
LXI D,DSTFCB
MVI A,1 ;Destination is always A
STAX D
PUSH D
MVI C,19
CALL BDOS ;Delete old file if present
POP D
MVI C,22
CALL BDOS ;Make new file
INR A
LXI D,DDFERR
JZ EXIT ;Disk full
POP H ;Restore pointer
LXI D,15
DAD D ;Point to last cluster
MOV E,M
INX H
MOV D,M
INX H
XCHG ;Save next cluster
SHLD CLUSTR
XCHG ;Get file size
MOV E,M
INX B
MOV D,M
INX H
MOV A,M
LXI H,7FH ;Convert to logical records
DAD D
ACI 0
DAD H
MOV L,H
MOV H,A ;Record count in HL
LXI D,DATBUF ;Buffer pointer in DE
MVI C,8 ;Buffer records in C
LOOP: MOV L,ORA
JNZ MORE ;More records in file
CALL FLUSH ;Flush data buffer
LXI D,DSTFCB
MVI C,16
CALL BDOS ;Close file
JMP BOOT ;Done
MORE: PUSH B ;Save parameters
PUSH H
PUSH D
LDA CLMASK ;Get mask
ANI C
JNZ CURRNT ;Disk and track current
LHLD CLUSTR
XRA A
MOV A,H
RAR
MOV D,A
RAR
MOV A,L
RAR
MOV E,A
PUSH PSM ;Save odd/even status
DAD D
LXI C,FAT
DAD D ;HL point at next cluster
MOV E,M
INX H ;DE have next cluster number
MOV D,M
POP PSM ;Bit count
MVI C,4 ;Previous cluster was odd
ODD: MOV A,D
ANI 0FH ;Keep only lowest 12 bits
MOV D,A
JMP UPDATE
ODD: XRA A ;Clear carry
MOV A,D ;Keep highest 12 bits
RAR
MOV D,A
RAR
MOV A,E
RAR
MOV E,A
DCR C
JNZ ODD ;Get current cluster
UPDATE: LHLD CLUSTR ;Replace with next cluster
XCHG
SHLD CLUSTR
LHLD CLOFF
MVI H,0
XCHG
DAD H ;Cluster*2
DAD D ;Compute track/sector from BL
LDA SPT
CMA
INR A
MOV E,A
MVI D,0FFH
MOV C,D
DIVIDE: DAD D ;Divide HL by spt
INR C ;Track in C
JC DIVIDE
LDA CLMASK
INR A
RRC

```

continued

## Listing 2, continued

```

RRC      B,A
MOV      A,L
SUB      E          ;Remainder in A
MULT:   ADD      A          ;Multiply by mask+1
MOV      E,A
MOV      A,B
RRC      B,A
MOV      A,E
JMC     MULT
IFR      A          ;First sector in #1
STA     SECTOR    ;Update sector
MOV      A,C
STA     TRACK     ;Update track
CALL    SETTRK   ;Set new track
MVI     C,1
CALL    SELDSK   ;Select next sector
CURRENT: LDA     SECTOR
CPI     37       ;No track overflow
JC      NOOVP
LDA     TRACK
IFR      A
MOV      C,A
CALL    SETTRK   ;Go to next track
MVI     A,1      ;Start with sector 1
NOOVP:  MOV      C,A
IFR      A
STA     SECTOR
CALL    SETSEC   ;Set next DMA address
POP      B
PUSH    SPTDMA
CALL    READ     ;Set next DMA address
ORA     A
JNZ     BOOT     ;Read error
POP      D
LXI     H,128
DAD     D
XCHG   POP      H
DCX     H
POP      B
IFR      C
CM      FLUSH    ;Flush data buffer if 128
JMP     LOOP
FLUSH:  INR      C
DCR     C
RZ      C        ;Buffer empty
PUSH    H
PUSH    B
MVI     C,8
CALL    SELDSK
POP      B
LXI     D,DATBUF
PUSH    D
FLUSH1: PUSH    B
PUSH    D
MVI     C,26
CALL    BDOS     ;Set DMA address
LXI     D,DSTPCB
MVI     C,21
CALL    BDOS     ;Write the record
LXI     D,DDFERR
ORA     A
JNZ     EXIT     ;Disk full
POP      D
POP      B
LXI     H,128
DAD     D
XCHG   POP      C
DCR     FLUSH1
JNZ     DDFERR
POP      H
RET
EXIT:   MVI     C,9
CALL    BDOS     ;Display message
JMP     BOOT     ;Reboot
SELDK:  JMP     001BH ;Values are filled in
SETTRK: JMP     001EH
SETSEC: JMP     0021H
SPTDMA: JMP     0024H
READ:   JMP     0027H
;
FWTERR: DB     '*** UNREADABLE PCDOS FORMAT ***'
DB     0DH,0AH,07H,'$'
FWFERR: DB     '*** FILE NOT FOUND ***',0DH,0AH,07H,'$'
DDFERR: DB     '*** DISK OR DIRECTORY FULL ***'
DB     0DH,0AH,07H,'$'
;
SPT:    DS     1 ;2*Sectors/track
CLOFF:  DS     1 ;2*Cluster offset
CLMASK: DS     1 ;Cluster mask
CLUSTER: DS    2 ;Next cluster
TRACK:  DS     1 ;Current logical track
SECTOR: DS     1 ;Next logical sector
STACK  DS     64 ;Stack area
STACK  EQU    $
;
ORG     ($+0FFF) AND 0FFF0H
;
FAT:    DS     1*200H ;File allocation table
DIRBUF: DS     7*200H ;PCDOS directory
DATBUF: DS     4000H ;Data buffer
;
END

```

## Customer Support Survey

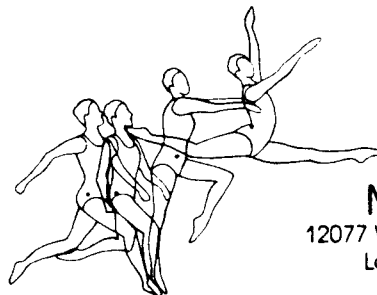
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## MicroMotion

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- Includes all file primitives described in Kernigan and Plauger's *Software Tools*.
- The input and output streams are fully redirectable.
- The editor, assembler and screen copy utilities are provided as relocatable object modules. They are brought into the dictionary on demand and may be released with a single command.
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- The string-handling package is the finest and most complete available.
- A listing of the nucleus is provided as part of the documentation.
- The language implementation exactly matches the one described in *FORTH TOOLS*, by Anderson & Tracy. This 200 page tutorial and reference manual is included with MasterFORTH.
- Floating Point & HIRES options available.
- Available for APPLE II/II+/IIE & CP/M 2.x users.
- MasterFORTH — \$100.00. FP & HIRES — \$40.00 each
- Publications
  - FORTH TOOLS — \$20.00
  - 83 International Standard — \$15.00
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# WRITE YOUR OWN THREADED LANGUAGE

by Douglas Davidson

The FORTH language presents a method remarkable for its simplicity, economy, and power; it should be remembered, however, that FORTH proper is but one example of the method referred to as *threaded language*. The characteristics of threaded languages make them particularly useful to hobbyists and all those who like to get close to the machine they are working with; it is my contention that the project of writing such a language is useful, educational, very much in the spirit of the language, and at the same time not very difficult. I will present in these articles a practical guide to the writing of one particular threaded language with the intention that it be customized and altered at will. This language is very similar to FORTH, but varies from it in a number of ways for the purposes of simplification.

A threaded language consists essentially of a collection of tools and some facilities for using and adding to these tools. The basic tools are simple routines to do things such as simple arithmetic operations, input and output, etc. The tools communicate by means of a LIFO (last in, first out) stack which forms the heart of the apparatus; most routines are defined in terms of their effects on the stack, and arithmetic operations are presented in RPN form (for an explanation of RPN, see the tint box on page 30.) The power of the language comes from its extensibility: new routines are defined in terms of old ones, and then become part of the tool collection, and can in turn be used in the definition of still more routines. This is the origin of the term "threaded:" routines are stored essentially as lists of references to other routines, which are "threaded" together. Before introducing specifics, I would like to present a list of definitions.

- **Word:** A named routine, consisting of a header followed by machine language code or data of some sort. See Figure 1.
- **Primary:** A word written in machine language; more generally, a word without a higher-level definition.
- **Secondary:** A word defined in higher-level terms—that is, in terms of other words. In this presentation the distinction between primary and secondary will be somewhat blurred by the fact that secondaries will actually consist of machine code, but this is not always the case, and the difference will

still be clear.

- **Dictionary:** The linked list of words. Words will be stored one after the other in memory; each one will contain a link to the previous one, and a record will be kept of the location of the last one.
- **Header:** The housekeeping information at the head of a word, here consisting only of the word's name and a link to the previous word in the dictionary. The name will be stored as its first three characters in ASCII form, preceded by its length—this is somewhat standard, and should be sufficient. The link follows the name and is two bytes, the NFA of the previous word.
- **NFA:** The name field address of a word—the address of the first byte of the header.
- **LFA:** The link field address of a word—the address of the fifth byte of the header, equal to NFA + 4.
- **PFA:** The parameter field address of a word—the address of the first byte following the header, equal to NFA + 6.

I wish to present the language from the bottom up; I will start with the simplest routines, the ones that must be coded first, and proceed through the more complex, developing details as needed. The routines will be presented in several ways—a functional description will be given in the text, and the 6502 assembly and machine code for an Apple II implementation will follow. The presentation here may be conformed to on at least four different levels: the machine code level, preserving all memory locations, and using an Apple; the assembly level, for another 6502 computer; the logic of the routines, translated into a different assembly language; or the functional descriptions of the routines. Obviously, it will be more of a personal language and easier to customize if it conforms less strictly to what is presented here, but the choice is yours. What is presented here is a bare-bones version, with all of the interfaces specified and the bugs ironed out. The memory map, at least for now, will be relatively simple. The dictionary will start near the bottom of memory and grow up; the stack will start near the top of memory (some room will be needed above it) and grow down; see Figure 2. Some space will also be needed for system variables. We will need a two-byte variable, S, to point to the head of the stack; as

each stack entry will consist of two bytes, S will be incremented or decremented in multiples of two. I now postpone details of more complex things to get right to some basic routines.

The first necessity is a

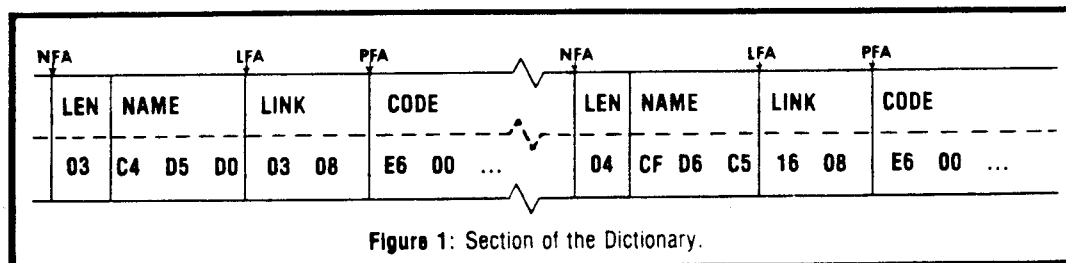


Figure 1: Section of the Dictionary.

start-up routine, but since we do not yet know all that needs to be done, it would be best to simply put a jump instruction at the start of the program and leave its destination for later. Immediately after that we start adding words to the dictionary; each consists of a header—one byte of name length, three bytes of name, and two bytes of link—followed by the machine code, ended with a return instruction. The link of the first word should be zero.

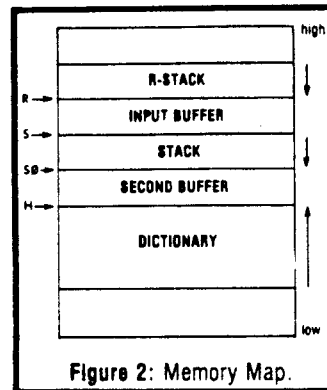


Figure 2: Memory Map.

### Stack Manipulation:

**DROP** removes the top stack element; it simply increments  $S$  by two.

**DUP** duplicates the top stack element; it decrements  $S$  by two, then moves the two bytes starting at  $S+2$  to the two bytes starting at  $S$ .

**OVER** places a copy of the second stack entry on top of the stack; it decrements  $S$  by two, then moves the two bytes starting at  $S+4$  to the two bytes starting at  $S$ .

**SWAP** exchanges the top two stack elements; it exchanges the two bytes starting at  $S$  with the two bytes starting at  $S+2$ .

**ROT** cyclically exchanges the top three stack elements; it exchanges the two bytes starting at  $S+2$  with the two at  $S+4$ , then the two at  $S$  with the two at  $S+2$ .

**> R** It will be useful for several reasons to maintain a second stack, the "return" stack, similar to but smaller than the first, and starting at the top of available memory and growing down. A two-byte variable,  $R$ , will point to the head of the return stack. The word **> R** moves the head of the main stack to the return stack; it decrements  $R$  by two, moves the two bytes at  $S$  to the two at  $R$ , and increments  $S$  by two.

**R>** This word is the opposite of **> R**; it decrements  $S$  by two, moves the two bytes at  $R$  to the two at  $S$ , then increments  $R$  by two.

**I** copies the head of the return stack to the main stack; it decrements  $S$  by two, then moves the two bytes at  $R$  to the two at  $S$ .

### Comparison:

**0=** We will use a "flag" to indicate logical values;  $\$0001$  = true,  $\$0000$  = false. All comparison operators will return these values, but for other purposes any non-zero value will be considered true. Also, it is conventional for words to destroy their operands; thus, the word **0** checks the value at the head of the stack and replaces it with a true flag if it is zero, or a false flag otherwise.

**0<** Stack values will be considered for different purposes as logical values, as two's complement values, as ASCII values, or as unsigned binary values. The word **0<** takes the top stack value as a two's complement signed integer; it

replaces the top stack entry with a true flag if its most significant bit is high, otherwise with a false flag.

**=** Words, as I have said, destroy their operands; the **=** word determines a flag, a true flag if the top two stack entries (i.e., the two bytes at  $S$  and the two bytes at  $S+2$ ) are equal and a false flag otherwise, then increments  $S$  by two and replaces the two bytes starting at  $S$  by the flag previously determined.

**<** considers the two top stack entries as two's complement signed binary integers and determines a flag, true if the first one (the two bytes starting at  $S+2$ ) is less than the second (the two bytes starting at  $S$ ) and false otherwise, then increments  $S$  and replaces the two bytes starting at  $S$  with the flag previously determined. **>** is similar to **<**, if "less than" is replaced by "greater than".

### Logical:

**AND** forms this bitwise logical AND of the two bytes starting at  $S$  with the two bytes starting at  $S+2$ , increments  $S$  by two, then replaces the two bytes starting at  $S$  with the result of the logical operation.

**OR** is similar to **AND**, but the operation is an OR.

**XOR** is similar to **AND**, but the operation is an exclusive-or.

**NOT** replaces the two bytes starting at  $S$  with their logical complement.

### Arithmetic:

**+** finds the sum of the two top stack entries, increments  $S$  by two, and replaces the two bytes starting at  $S$  with the sum.

**-** is similar to **+**, but the difference rather than the sum is calculated; note that no overflow checking is performed.

**NEGATE** replaces the top stack entry by its two's complement additive inverse; essentially it exclusive-ors the two bytes with  $\$FFFF$  and then increments them by one.

**ABS** replaces the top stack entry by its absolute value; if the MSB is high, it calls **NEGATE**, otherwise it does nothing.

**\*** It is wise, for the multiplication and division words, to reserve about ten bytes for accumulators, and to have headerless routines (a) to move stack values into these accumulators, taking their absolute values first and saving the final sign elsewhere, (b) to move a value from the accumulator to the stack, giving it the saved sign, and (c) to perform operations on the accumulators. The **\*** word takes the two top stack entries, considered as two's complement binary integers, removes them from the stack, forms their product, and places it on the stack.

**/** is similar to **\***, but it forms the quotient (of the first value divided by the second) rather than the product.

**/MOD** considers the two top stack values as unsigned binary integers, takes them off the stack, forms their quotient and remainder, and puts first the remainder, then the quotient on the stack.

**MOD** is similar to **/MOD**, but it discards the quotient and returns just the remainder.

**\*/** takes the three top stack entries, considered as two's



complement binary integers, off the stack, forms the 32-bit product of the first two, and divides this 32-bit product by the third. It then places the resulting 16-bit value back on the stack.

**\*/MOD** is similar to **\*/**, but it considers the entries as unsigned binary values, and it returns first a remainder and then a quotient.

**Memory:**

**!** takes the value in the two bytes starting at **S+2** and stores it in the two-byte location pointed to by the two bytes starting at **S**; it then increments **S** by four.

**+!** takes the value in the two bytes starting at **S+2** and adds it to the two-byte value pointed to by the two bytes starting at **S**, then stores the sum in the location pointed to by the two bytes starting at **S**; it then increments **S** by four.

**C!** takes the value in the one byte starting at **S+2** and stores it in the one byte pointed to by the two bytes starting at **S**; it then increments **S** by four.

**@** replaces the two bytes starting at **S** with the two bytes they point to.

**C@** replaces the two bytes starting at **S** with the one byte they point to and a **\$00** for the upper byte.

The next installment will present more complex routines, including most of the input-output and dictionary management. For now, test each of these simple routines independently, and perhaps add some more—anyone familiar with **FORTH** will know several more. The purpose of some of these routines will become clearer as things progress.

```

*****
** CODE FOR SAMPLE THREADED LANGUAGE **
** APPLE/11650? **
*****
0000: 4c 16 13 JMF STARTUP
*
** DROP **
*
0003: 04 C4 D2 CF 00 00 INC SL ; increment S by 2
0009: E6 00 BNE OK1
000B: D0 02 BNE OK1
000D: E6 01 INC SH
000F: E6 00 OK1 INC SL
0011: D0 02 BNE OK2
0013: E6 01 INC SH
0015: 60 RTS
*
** DUP **
*
0016: 03 C4 D5 D0 03 00 INC SL ; decrement S by 2
001E: C6 00 DEC SL
0020: D0 02 BNE OK1
0022: C6 01 DEC SH
0024: C6 00 OK1 DEC SL
0026: D0 02 BNE OK2
0028: C6 01 DEC SH
002A: C6 00 OK2 DEC SL
002C: A0 03 LDY 0003 ; move the two bytes
002E: B1 00 LDA (S),Y ; at S+2
0030: A0 01 LDY 0001 ; to the two bytes
0032: 91 00 STA (S),Y ; at S
0034: C8 INY
0035: B1 00 LDA (S),Y
0037: A0 00 LDY 0000
0039: 91 00 STA (S),Y
003B: 60 RTS
*
** OVER **
*
003C: 04 CF D6 C5 16 00 INC SL ; decrement S by 2
0042: E6 00 DEC SL
0044: C6 00 BNE OK1
0046: D0 02 BNE OK1
0048: C6 01 DEC SH
004A: C6 00 OK1 DEC SL
004C: D0 02 BNE OK2
004E: C6 01 DEC SH
0050: C6 00 OK2 DEC SL
0052: A0 05 LDY 0005 ; move the two bytes
0054: B1 00 LDA (S),Y ; at S+4
0056: A0 01 LDY 0001 ; to the two bytes
0058: 91 00 STA (S),Y ; at S
005A: A0 04 LDY 0004
005C: B1 00 LDA (S),Y
005E: A0 00 LDY 0000
0060: 91 00 STA (S),Y
0062: 60 RTS

```

```

*
** SWAP **
*
0063: 04 D3 D7 C1 3C 00 LDY 0003 ; exchange the two
0069: A0 03 LDA (S),Y ; bytes
006B: B1 00 LDA (S),Y ; at S+2 with
006D: AA TAX ; the two bytes at S
006E: A0 01 LDY 0001
0070: B1 00 LDA (S),Y
0072: A0 03 LDY 0003
0074: 91 00 STA (S),Y
0076: A0 01 LDY 0001
0078: 9A TYA
0079: 91 00 STA (S),Y
007B: C8 INY
007C: B1 00 LDA (S),Y
007E: AA TAX
007F: A0 00 LDY 0000
0081: B1 00 LDA (S),Y
0083: A0 02 LDY 0002
0085: 91 00 STA (S),Y
0087: A0 00 LDY 0000
0089: 9A TYA
008A: 91 00 STA (S),Y
008B: 60 RTS
*
** ROT **
*
008D: 03 D2 CF D4 63 00 INC SL ; swap the two bytes
0093: E6 00 BNE OK1 ; at S+4 with the
0095: D0 02 BNE OK1 ; two bytes at S+2
0097: E6 01 INC SH
0099: E6 00 OK1 INC SL
009B: D0 02 BNE OK2
009D: E6 01 INC SH
009F: 20 69 00 D0 2 JSR SWAP
00A2: E6 00 INC SL ; then swap the two
00A4: C6 00 DEC SL ; bytes at S+2
00A6: D0 02 BNE OK3 ; with the two bytes
00A8: C6 01 DEC SH ; at S
00AA: C6 00 OK3 DEC SL
00AC: D0 02 BNE OK4
00AE: C6 01 DEC SH
00B0: C6 00 OK4 DEC SL
00B2: 4C 69 00 JMF SWAP
*
** >R **
*
00B5: 02 BE D2 A0 0D 00 INC RL ; decrement R by 2
00BB: E6 02 DEC RL
00BD: C6 02 BNE OK1
00BF: D0 02 BNE OK1
00C1: C6 03 DEC RH
00C3: C6 02 OK1 DEC RL
00C5: D0 02 BNE OK2
00C7: C6 03 DEC RH
00C9: C6 02 OK2 DEC RL
00CB: A0 01 LDY 0001 ; move the two bytes
00CD: B1 00 LDA (S),Y ; at S to the
00CF: 91 02 STA (R),Y ; two bytes at R
00D1: 88 DEY
00D3: B1 00 LDA (S),Y
00D5: 91 02 STA (R),Y
00D7: E6 00 INC SL ; increment S by 2
00D9: D0 02 BNE OK3
00DB: E6 01 INC SH
00DD: E6 00 OK3 INC SL
00DE: D0 02 BNE OK4
00E0: E6 01 INC SH
00E2: 60 RTS
*
** R **
*
00E3: 02 D2 BE A0 B5 00 INC SL ; decrement S by 2
00E9: E6 00 DEC SL
00EB: C6 00 BNE OK1
00ED: D0 02 BNE OK1
00EF: C6 01 DEC SH
00F1: C6 00 OK1 DEC SL
00F3: D0 02 BNE OK2
00F5: C6 01 DEC SH
00F7: C6 00 OK2 DEC SL
00F9: A0 01 LDY 0001 ; move the two bytes
00FB: B1 02 LDA (R),Y ; at R to the
00FD: 91 00 STA (S),Y ; two bytes at S
00FF: 88 DEY
0100: B1 02 LDA (R),Y
0102: 91 00 STA (S),Y
0104: E6 02 INC RL ; increment R by 2
0106: D0 02 BNE OK3
0108: E6 03 INC RH
010A: E6 02 OK3 INC RL
010C: D0 02 BNE OK4
010E: E6 03 INC RH
0110: 60 OK4 RTS
*
** I **
*
0111: 01 C9 A0 A0 E3 00 INC SL ; decrement S by 2
0117: E6 00 DEC SL
0119: D0 02 BNE OK1
011B: D0 02 BNE OK1
011D: C6 01 DEC SH
011F: C6 00 OK1 DEC SL
0121: D0 02 BNE OK2
0123: C6 01 DEC SH
0125: C6 00 OK2 DEC SL
0127: A0 01 LDY 0001 ; move the two bytes
0129: B1 02 LDA (R),Y ; at R to the
012B: 91 00 STA (S),Y ; two bytes at S
012D: 88 DEY
012E: B1 02 LDA (R),Y
0130: 91 00 STA (S),Y
0132: 60 RTS
*
** 0= **
*
0133: 02 00 BD A0 11 09 LDY 0000 ; are the two bytes
0139: A0 00 LDA (S),Y ; at S both zero?
013B: B1 00 BNE NZ
013D: D0 00 BNE NZ
013F: C8 INY
0140: B1 00 LDA (S),Y
0142: D0 03 BNE NZ
0144: 98 TYA ; yes, flag=0001

```

continued

```

0945: D0 02      BNE ZERO
0947: A9 00      NZ      LDA #000
0949: A0 00      ZERO     LDY #000
094B: 91 00      STA (S),Y
094D: 9B          TYA
094E: CB          INY
094F: 91 00      STA (S),Y
0951: 60          RTS
*
** @C **
*
0952: 02 B0 BC A0 33 09 LDY #001 ; is the MSB high?
0958: A0 01      LDA (S),Y
095A: B1 00      BMI MINUS
095C: 30 01      DEY ; no, flag=0000
095E: 80          DEY ; yes, flag=0001
095F: 9B          MINUS   LDY #000
0960: A0 00      LDA (S),Y
0962: 91 00      STA (S),Y
0964: 9B          TYA
0965: CB          INY
0966: 91 00      STA (S),Y
0968: 60          RTS
*
** = **
*
0969: 01 B0 A0 A6 52 09 LDY #000 ; are the two bytes
096F: A0 00      LDA (S),Y ; at S equal to the
0971: B1 00      BNE #000 ; two bytes at S+2?
0973: A0 02      LDY #002
0975: D1 00      CMP (S),Y
0977: D0 0D      BNE NEG
0979: 80          DEY
097A: B1 00      LDA (S),Y
097C: A0 03      LDY #003
097E: D1 00      CMP (S),Y
0980: D0 04      BNE NEG
0982: A9 01      LDA #001 ; yes, flag=0001
0984: D0 0C      BNE EQ
0986: A9 00      LDA #000 ; no, flag=0000
0988: A0 02      EQ      LDY #002
098A: 91 00      STA (S),Y
098C: CB          INY
098D: A9 00      LDA #000
098F: 91 00      STA (S),Y
0991: E6 00      INC SL ; increment S by 2
0993: D0 02      BNE OK1
0995: E6 01      INC SH
0997: E6 00      OK1    INC SL
0999: D0 02      BNE OK2
099B: E6 01      INC SH
099D: 60          RTS
*
** < **
*
099E: 01 BC A0 A0 69 09 LDY #002 ; compare the two bytes
09A4: A0 02      LDA (S),Y ; at S+2 with the
09A6: 3B          SEC ; two bytes at S
09A7: B1 00      LDA (S),Y
09A9: A0 00      LDY #000
09AB: F1 00      SBC (S),Y
09AD: A0 03      LDY #003
09AF: B1 00      LDA (S),Y
09B1: A0 01      LDY #001
09B3: F1 00      SBC (S),Y
09B5: 50 02      BVC #1
09B7: 49 00      EOR #000
09B9: 29 00      OK1    AND #000
09BB: 0A          ASL
09BC: 2A          ROL ; and produce a flag
09BD: CB          INY
09BE: 91 00      STA (S),Y
09C0: A9 00      LDA #000
09C2: CB          INY
09C3: 91 00      STA (S),Y
09C5: E6 00      INC SL ; increment S by 2
09C7: D0 02      BNE OK2
09C9: E6 01      INC SH
09CB: E6 00      OK2    INC SL
09CD: D0 02      BNE OK3
09CF: E6 01      INC SH
09D1: 60          OK3    RTS
*
** > **
*
09D2: 01 BE A0 A0 9E 09 LDY #000 ; compare the two bytes
09D8: A0 00      LDA (S),Y ; at S with the two
09DA: 3B          SEC ; bytes at S+2
09DB: B1 00      LDA (S),Y
09DD: A0 02      LDY #002
09DF: F1 00      SBC (S),Y
09E1: 80          DEY
09E2: B1 00      LDA (S),Y
09E4: A0 03      LDY #003
09E6: F1 00      SBC (S),Y
09E8: 50 02      BVC OK1
09EA: 49 00      EOR #000
09EC: 29 00      OK1    AND #000
09EE: 0A          ASL
09EF: A9 00      LDA #000
09F1: 91 00      STA (S),Y
09F3: 80          DEY
09F4: 2A          ROL ; and produce a flag
09F5: 91 00      STA (S),Y
09F7: E6 00      INC SL ; increment S by 2
09F9: D0 02      BNE OK2
09FB: E6 01      INC SH
09FD: E6 00      OK2    INC SL
09FF: D0 02      BNE OK3
0A01: E6 01      INC SH
0A03: 60          OK3    RTS
*
** AND **
*
0A04: 03 C1 CE C4 D2 09 LDY #000 ; AND the two bytes
0A0A: A0 00      LDA (S),Y ; starting at S with
0A0C: B1 00      LDA (S),Y ; the two at S+2
0A0E: A0 02      LDY #002
0A10: 31 00      AND (S),Y
0A12: 91 00      STA (S),Y
0A14: 80          DEY
0A15: B1 00      LDA (S),Y
0A17: A0 03      LDY #003
0A19: 31 00      AND (S),Y
0A1B: 91 00      STA (S),Y

```

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0A1D: E6 00      INC SL ; increment S by 2
0A1F: D0 02      BNE OK1
0A21: E6 01      INC SH
0A23: E6 00      OK1    INC SL
0A25: D0 02      BNE OK2
0A27: E6 01      INC SH
0A29: 60          OK2    RTS
*
** OR **
*
0A2A: 02 CF D2 A0 04 0A LDY #000 ; OR the two bytes
0A30: A0 00      LDA (S),Y ; starting at S
0A32: B1 00      LDA (S),Y ; with the two at S+2
0A34: A0 02      LDY #002
0A36: 11 00      ORA (S),Y
0A38: 91 00      STA (S),Y
0A3A: 80          DEY
0A3B: B1 00      LDA (S),Y
0A3D: A0 03      LDY #003
0A3F: 11 00      ORA (S),Y
0A41: 91 00      STA (S),Y
0A43: E6 00      INC SL ; increment S by 2
0A45: D0 02      BNE OK1
0A47: E6 01      INC SH
0A49: E6 00      OK1    INC SL
0A4B: D0 02      BNE OK2
0A4D: E6 01      INC SH
0A4F: 60          OK2    RTS
*
** XOR **
*
0A50: 03 D6 CF D2 2A 0A LDY #000 ; XOR the two bytes
0A56: A0 00      LDA (S),Y ; starting at S with
0A58: B1 00      LDA (S),Y ; the two at S+2
0A5A: A0 02      LDY #002
0A5C: 51 00      EOR (S),Y
0A5E: 91 00      STA (S),Y
0A60: 80          DEY
0A61: B1 00      LDA (S),Y
0A63: A0 03      LDY #003
0A65: 51 00      EOR (S),Y
0A67: 91 00      STA (S),Y
0A69: E6 00      INC SL ; increment S by 2
0A6B: D0 02      BNE OK1
0A6D: E6 01      INC SH
0A6F: E6 00      OK1    INC SL
0A71: D0 02      BNE OK2
0A73: E6 01      INC SH
0A75: 60          OK2    RTS
*
** NOT **
*
0A76: 03 CE CF D4 50 0A LDY #001 ; take the complement
0A7C: A0 01      LDA (S),Y ; of the two bytes
0A7E: B1 00      LDA (S),Y ; starting at S
0A80: 49 FF      EOR #FFF
0A82: 91 00      STA (S),Y
0A84: 80          DEY
0A85: B1 00      LDA (S),Y
0A87: 49 FF      EOR #FFF
0A89: 91 00      STA (S),Y
*
** + **
*
0A8C: 01 AB A0 A0 76 0A LDY #000 ; add the two bytes
0A92: 1B          SEC ; starting at S with
0A93: A0 00      LDA (S),Y ; the two at S+2
0A95: B1 00      LDA (S),Y
0A97: A0 02      LDY #002
0A99: 71 00      ADC (S),Y
0A9B: 91 00      STA (S),Y
0A9D: 80          DEY
0A9E: B1 00      LDA (S),Y
0AA0: A0 03      LDY #003
0AA2: 71 00      ADC (S),Y
0AA4: 91 00      STA (S),Y
0AA6: E6 00      INC SL ; increment S by 2
0AA8: D0 02      BNE OK1
0AAA: D0 02      INC SH
0AAC: E6 00      OK1    INC SL
0AAE: D0 02      BNE OK2
0AB0: E6 01      INC SH
0AB2: 60          OK2    RTS
*
** - **
*
0AB3: 01 AD A0 A0 BC 0A LDY #000 ; subtract the two bytes
0AB9: 3B          SEC ; starting at S from
0ABA: A0 02      LDA (S),Y ; the two at S+2
0ABC: B1 00      LDA (S),Y
0ABE: A0 00      LDY #000
0AC0: F1 00      SBC (S),Y
0AC2: A0 02      LDY #002
0AC4: 91 00      STA (S),Y
0AC6: CB          INY
0AC7: B1 00      LDA (S),Y
0AC9: A0 01      LDY #001
0ACB: F1 00      SBC (S),Y
0ACD: A0 03      LDY #003
0ACF: 91 00      STA (S),Y
0AD1: E6 00      INC SL ; increment S by 2
0AD3: D0 02      BNE OK1
0AD5: E6 01      INC SH
0AD7: E6 00      OK1    INC SL
0AD9: D0 02      BNE OK2
0ADB: E6 01      INC SH
0ADD: 60          OK2    RTS
*
** NEGATE **
*
0ADE: 06 CE C5 C7 B3 0A JSR NOT ; first take the complement
0AE4: 20 7C 0A      LDY #000 ; then increment the
0AE7: A0 00      LDA (S),Y ; two bytes starting at S
0AE9: B1 00      LDA (S),Y
0AEB: 1B          CLC
0AEC: 69 01      ADC #001
0AEE: 91 00      STA (S),Y
0AEF: 90 07      BCC DONE
0AF1: CB          INY
0AF3: B1 00      LDA (S),Y
0AF5: 69 00      ADC #000
0AF7: 91 00      STA (S),Y
0AF9: 60          DONE   RTS

```

continued

```

*
** ABS **
*
@AFA: @3 C1 C2 D3 DE @A
@B00: A0 @1 LDY #001 ; is the MSB high?
@B02: B1 @0 LDA (S),Y
@B04: 10 @3 BPL DONE
@B06: 4C E4 @A JMP NEGATE ; yes, negate
@B07: 60 RTS ; no, do nothing
*
** 16*16=32 **
*
No Header
@B0A: A9 @0 LDA #000 ; clear accumulators
@B0C: 85 12 STA ACC.B2L
@B0E: 85 13 STA ACC.B2H
@B10: 85 14 STA ACC.C1L
@B12: 85 15 STA ACC.C1H
@B14: 85 16 STA ACC.C2L
@B16: 85 17 STA ACC.C2H
@B18: 46 @F PASS LSR ACC.AH ; check a bit
@B1A: 66 @E ROR ACC.AL
@B1C: 90 19 BCC SHIFT ; branch if not set
@B1E: 10 CLC ; add if set
@B1F: A5 10 LDA ACC.B1L ; B+C -> C
@B21: 65 14 ADC ACC.C1L
@B23: 85 14 STA ACC.C1L
@B25: A5 11 LDA ACC.B1H
@B27: 65 15 ADC ACC.C1H
@B29: 85 15 STA ACC.C1H
@B2B: A5 12 LDA ACC.B2L
@B2D: 65 16 ADC ACC.C2L
@B2F: 85 16 STA ACC.C2L
@B31: A5 13 LDA ACC.B2H
@B33: 65 17 ADC ACC.C2H
@B35: 85 17 STA ACC.C2H
@B37: 06 10 SHIFT ASL ACC.B1L ; and shift B left
@B39: 26 11 ROL ACC.B1H
@B3B: 26 12 LDA ACC.B2L
@B3D: 26 13 ROL ACC.B2H
@B3F: A5 @E LDA ACC.AL ; until done
@B41: D0 D5 BNE PASS
@B43: A5 @F LDA ACC.AH
@B45: D0 D1 BNE PASS
@B47: 60 RTS
*
** 32/16=16 **
*
No Header
@B48: A9 @0 LDA #000 ; clear accumulators
@B4A: 85 14 STA ACC.C1L
@B4C: 85 15 STA ACC.C1H
@B4E: A2 10 LDX #10 ; # of passes
@B50: 06 10 PASS ASL ACC.B1L ; shift B left
@B52: 26 11 ROL ACC.B1H
@B54: 26 12 ROL ACC.B2L
@B56: 26 13 ROL ACC.B2H
@B58: 90 @C BCC NORMAL ; have we missed a bit?
@B5A: A5 12 LDA ACC.B2L ; yes, we must subtract
@B5C: E5 @E SBC ACC.AL ; no matter what
@B5E: 48 PHA
@B60: A5 13 LDA ACC.B2H
@B62: E5 @F SBC ACC.AH
@B64: A5 12 LDA ACC.B2L ; yes, we must subtract
@B66: E5 @E SBC ACC.AL ; no matter what
@B68: 48 PHA
@B6A: A5 13 LDA ACC.B2H
@B6C: E5 @F SBC ACC.AH
@B6E: 38 BCS SUB
@B70: 80 @C SEC
@B72: 38 NORMAL SEC ; normally we subtract
@B74: A5 12 LDA ACC.B2L ; only if the
@B76: difference
@B78: E5 @E SBC ACC.AL ; is positive
@B7A: 48 PHA
@B7C: A5 13 LDA ACC.B2H
@B7E: E5 @F SBC ACC.AH
@B80: 90 @2 BCC NOSUB1
@B82: 85 13 STA ACC.B2H
@B84: 08 PLA
@B86: 90 @2 BCC NOSUB2
@B88: 85 12 STA ACC.B2L
@B8A: 26 14 NOSUB2 ROL ACC.C1L ; shift the bit into
@B8C: 26 15 ROL ACC.C1H ; the quotient
@B8E: CA DEX
@B90: D0 D0 BNE PASS
@B92: 60 RTS
*
** 16*16=16 **
*
No Header
@B93: A9 @0 LDA #000 ; clear accumulator
@B95: 85 14 STA ACC.C1L
@B97: 85 15 STA ACC.C1H
@B99: 46 @F PASS LSR ACC.AH ; check bit
@B9B: 66 @E RFR ACC.AL
@B9D: 90 @D BCC NOADD
@B9F: 10 CLC ; it's set
@BA1: A5 10 LDA ACC.B1L ; therefore B+C -> C
@BA3: 65 14 ADC ACC.C1L
@BA5: 85 14 STA ACC.C1L
@BA7: A5 11 LDA ACC.B1H
@BA9: 65 15 ADC ACC.C1H
@BAB: 85 15 STA ACC.C1H
@BAC: 06 10 NOADD ASL ACC.B1L ; shift B left
@BAE: 26 11 ROL ACC.B1H
@BAF: A5 @E LDA ACC.AL ; if either A or B
@BB1: D0 @4 BNE NOPE ; is zero, we're done
@BB3: A5 @F LDA ACC.AH
@BB5: 08 BEO DONE
@BB7: A5 11 NOPE LDA ACC.B1H
@BB9: D0 D0 BNE PASS
@BBB: A5 10 LDA ACC.B1L
@BBD: D0 D9 BNE PASS
@BBE: 60 DONE RTS
*
** ->ACC **
*
No Header
@BBF: A0 @3 LDY #003 ; first save the
@BC1: B1 @0 LDA (S),Y ; final sign
@BC3: A0 @1 LDY #001
@BC5: 51 @0 EOR (S),Y
@BC7: 85 18 STA SCRL
@BC9: 20 @0 @B JSR ABS ; get the absolute
@BCB: A0 @1 LDY #001 ; value of the
@BCD: B1 @0 LDA (S),Y ; first number

```

```

STA ACC.AH
DEY
LDA (S),Y
STA ACC.AL
JSR DROP ; and that of
LDA #001 ; the second
LDA (S),Y
STA ACC.B1H
DEY
LDA (S),Y
STA ACC.B1L
RTS
*
** ACC-> **
*
No Header
@BCD: A0 @0 LDY #000 ; put back
@BCE: A5 14 LDA ACC.C1L ; the result
@BD1: 91 @0 STA (S),Y
@BD3: C8 INY
@BD5: A5 15 LDA ACC.C1H
@BD7: 91 @0 STA (S),Y
@BD9: A5 18 LDA SCRL ; with the
@BDB: 10 @3 BPL DONE ; proper sign
@BDD: 4C E4 @A JMP NEGATE
@BDE: 60 RTS
*
** * * *
*
@BDF: 01 AA A0 A0 FA @A JSR ->ACC
@BE1: 20 AF @B JSR 16*16=16
@BE3: 20 B1 @B JSR ACC->
*
** / **
*
@BE5: 01 AF A0 A0 EC @B JSR ->ACC
@BE7: 20 AF @B LDA #000 ; zero out the
@BE9: A9 @0 STA ACC.B2L ; rest of B
@BEB: 85 12 STA ACC.B2H
@BED: 20 4B @B JSR 32/16=16
@BEF: 4C D9 @B JMP ACC->
*
** /MOD **
*
@C01: 04 AF CD CF FB @B LDY #03 ; get the two
@C03: A0 @3 LDA (S),Y ; unsigned numbers
@C05: B1 @0 LOOP STA ACC.AL,Y
@C07: 99 @E @0 DEY
@C09: 88 BPL LOOP
@C0B: C8 INY ; clear out the
@C0D: 84 12 STY ACC.B2L ; rest of B
@C0F: 84 13 STY ACC.B2H
@C11: 20 4B @B JSR 32/16=16
@C13: A0 @F LDY #00 ; store the quotient
@C15: A5 14 MODISH LDA ACC.C1L
@C17: 91 @0 STA (S),Y
@C19: C8 INY
@C1B: A5 15 LDA ACC.C1H
@C1D: 91 @0 STA (S),Y ; and the remainder
@C1F: C8 INY
@C21: A5 12 LDA ACC.B2L
@C23: A5 12 STA (S),Y
@C25: 91 @0 INY
@C27: C8 LDA ACC.B2H
@C29: A5 13 STA (S),Y
@C2B: 91 @0 RTS
*
** MOD **
*
@C2D: 03 CD CF C4 10 @C LDY #03 ; get the two
@C2F: A0 @3 LDA (S),Y ; unsigned numbers
@C31: B1 @0 LOOP STA ACC.AL,Y
@C33: 99 @E @0 DEY
@C35: 88 BPL LOOP
@C37: 10 FB INY ; clear out the
@C39: 84 12 STY ACC.B2L ; rest of B
@C3B: 84 13 STY ACC.B2H
@C3D: 20 4B @B JSR 32/16=16
@C3F: E6 @F INC SL ; drop a value
@C41: D0 @2 BNE Dk1
@C43: E6 @1 INC SH
@C45: E6 @0 DA 1 INC SL
@C47: D0 @2 BNE Dk2
@C49: E6 @1 INC SH
@C4B: A0 @0 DA 2 LDY #00 ; and return just
@C4D: A5 12 LDA ACC.B2L ; the remainder
@C4F: 91 @0 STA (S),Y
@C51: C8 INY
@C53: A5 13 LDA ACC.B2H
@C55: 91 @0 STA (S),Y
@C57: 60 RTS
*
** * / **
*
@C59: 02 AA AF A0 3E @C JSR DROP ; first multiply
@C5B: 20 @9 @B JSR ->ACC ; the first two
@C5D: 20 AF @B JSR 16*16=32 ; numbers
@C5F: 20 @4 @B LDY #03 ; then move C -> B
@C61: A0 @3 LDA ACC.C1L,Y
@C63: 99 10 @A STA ACC.B1L,Y
@C65: 88 DEY
@C67: 10 F7 BPL LOOP
@C69: A5 @0 LDA SL ; and get the third
@C6B: 38 SEC ; number
@C6D: E9 @4 SBC #04
@C6F: 85 @4 STA SL
@C71: 80 @2 BCS Dk1
@C73: C6 @1 DEC SH
@C75: A0 @1 DA 1 LDY #01 ; with its sign
@C77: B1 @0 LDA (S),Y
@C79: A5 10 EOR SCRL
@C7B: 85 18 STA SCRL
@C7D: 20 @0 @B JSR ABS ; put its absolute
@C7F: A0 @1 LDY #001 ; value in A
@C81: B1 @0 LDA (S),Y
@C83: 85 @F STA ACC.AH
@C85: 88 DEY
@C87: B1 @0 LDA (S),Y
@C89: 85 @E STA ACC.AL
@C8B: 20 4B @B JSR 32/16=16 ; and divide by it
@C8D: 10 CLC ; drop the two

```

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# Interfacing Tips and Troubles

A Column by Neil Bungard

## Introduction

Every new column begins with a particular theme in mind. Perhaps an appropriate theme for "Interfacing Tips and Troubles" would be "get down to brass tacks and make the interface work." This column will take a practical and workable approach to connecting computers to the real world. We will look at the troubles which you will likely encounter when attempting to connect interface circuits to your computer, and we will review some handy tips which will make your interfacing tasks a little less work. As you may have already discovered, conceptualizing a circuit, creating a logic diagram, and wiring the circuit are only part of an interfacing task. Once all of these things have been done, you've still got to make the interface work. Sometimes you can connect your interface to the computer and it works the first time, but in many cases it does not. You may trace your circuit and find that it has been wired correctly, so you go back to the schematic diagram to see if you've made a logic error. Upon discovering that your logic was correct you disconnect the interface from the computer, connect wires to the buses and the control signal inputs of your circuit, and check the interface under static conditions. Surprisingly, it works! Where to next? That's part of what this column is all about—determining the source of problems which don't appear on the logic diagrams. Such problems can be caused by power supply noise, lack of sufficient (or proper) decoupling, improper cable termination, mismatched transfer timing, and a number of other conditions which are rarely discussed in interfacing literature. I will address a number of these issues myself and I hope to solicit help from you, the readers, who have encountered and solved such problems in your interfacing experiences.

Although the interfacing techniques are straightforward, each personal computer has its own unique idiosyncrasies which may add a "twist" to the interfacing process. As you interface your computer and discover its particular quirks, drop us a letter; we would like to share the benefits of your experience with others who own similar machines.

"Interfacing Tips and Troubles" also hopes to provide a number of helpful tips that will assist you in your interfacing tasks. These "tips" will range from software suggestions to trick circuits which will hopefully help you as you connect your computer to the real world. Here again, your experience can be of benefit to us. Everybody has a trick which has made interfacing a little easier for you. Drop us a line; we would like to share your trick with others.

## DC to DC Converter

We will begin this column with a handy little circuit which

eliminates the need for multiple output power supplies in applications where the supply current requirements are low. Some of the applications for such a circuit include: voltage levels for the RS 232 serial interface, programming voltages for EPROMs and CPUs, voltage references for analog to digital converters, etc. Typically, if a circuit requires more than one voltage, a multiple output power supply is used. A few disadvantages of the multiple output power supply are that it is physically large, relatively expensive, and in many cases is hard to find for the specific voltages that you are interested in. Another problem is adding ICs that require voltages other than five volts to a circuit with only a five volt power supply. At this point, if you are going to use a multiple output power supply, you must replace the existing supply. Of course, you would like to avoid that if possible.

I have managed to avoid multiple output power supplies in many applications by using a little circuit shown to me by Cam "Cannonball" Reid. Cam is always good for a trick circuit when I need one. This circuit is a DC to DC converter that you can build and place right on the board to generate needed voltage levels. A general circuit diagram of the DC to DC converter is shown in Figure 1. NPN transistors Q1

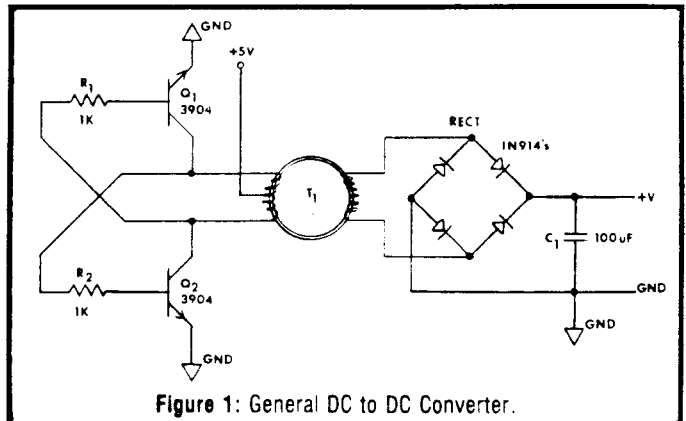


Figure 1: General DC to DC Converter.

and Q2, resistors R1 and R2, and the primary of transformer T1 form an astable multivibrator. The frequency of the multivibrator is somewhat dependent upon the physical characteristics of T1, but in general it will oscillate at about 1000hz. As the multivibrator oscillates, it induces a voltage into the secondary of T1. The voltage in the secondary winding is stepped up according to the relationship:

$$V_S = \frac{N_S}{N_P} \times V_P$$

$V_S$  = Voltage Secondary  
 $V_P$  = Voltage Primary  
 $N_S$  = Turns Secondary  
 $N_P$  = Turns Primary

A bridge rectifier converts the secondary oscillation to an unfiltered direct current and capacitor C1 smooths the waveform. Since the frequency of the unfiltered DC is relatively high (compared to 120hz for a conventional power supply), capacitor C1 can be small (about 100mf). As shown in the photograph in Figure 2, the DC to DC converter can be made very small so that little board space will be dedicated to accomplishing your voltage conversion.

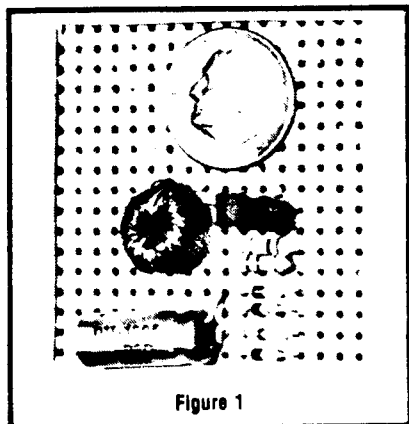


Figure 1

This DC to DC converter can be used to generate either a positive or a negative voltage by simply connecting the appropriate leg of the bridge rectifier to ground. Development of the DC to DC converter can be carried further to incorporate a three terminal voltage regulator (like the 7905) to ensure a stable voltage level. A plus and minus output is also possible from the DC to DC converter. By center tapping the secondary winding and connecting the center tap to ground, a positive voltage can be obtained from one leg of the bridge rectifier and a negative voltage can be obtained from the other leg. Circuits representing these applications will be presented in the following discussions.

The following circuits represent a couple of applications for which I have personally found the DC to DC converter useful. In the first circuit (Figure 3), the DC to DC converter was used to generate the programming voltage for a 2716 EPROM. It was very important that the programming voltage did not exceed 25 volts, so the output of the supply was regulated with a zener diode. The circuit in Figure 3 works exactly like the general DC to DC converter circuit in Figure 1. T1, a toroidal core transformer, can be purchased from Mouser Electronics for about a dollar, and they can be ordered in various sizes. The size (in inches) used in the converter above was: 0.50 (outside diameter) by 0.30 (inside diameter) by 0.19 (height). The primary winding consists of about 20 turns of number 26 enameled copper wire. The number of turns on the secondary winding was calculated according to the equation:

$$N_s = \frac{V_s}{V_p} \times N_p$$

These windings were then placed on the core and T1 was wired into the converter circuit. The converter circuit was to be regulated at 25 volts under a loaded condition so that the unregulated voltage was adjusted to about 26.5 volts. To adjust the unregulated output, remove the zener diode from the circuit, place a voltmeter on the secondary of T1 until the desired voltage is obtained. Once the 26.5 volts is obtained, place the zener diode back into the circuit—the DC to DC converter is now ready for service.

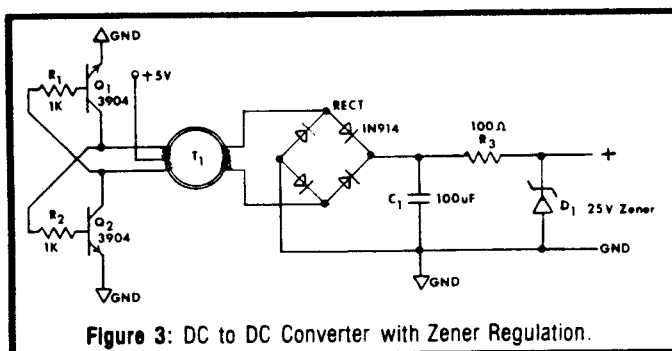


Figure 3: DC to DC Converter with Zener Regulation.

The circuit in Figure 4 is an example of generating a negative 12 volt reference using the DC to DC converter and a standard three terminal voltage regulator (7912). Before adjusting the secondary voltage, consult the specifications for the particular regulator that you are using. These three terminal regulators require a minimum input to output voltage difference to operate properly. Also keep in mind that the voltage difference between the input and the output will be dropped across the voltage regulator and dissipated as heat, so stay as close to the minimum difference specification as possible. The capacitors, C2 and C3, on either side of the voltage regulator in Figure 4 ensure that oscillations do not occur within the voltage regulator itself.

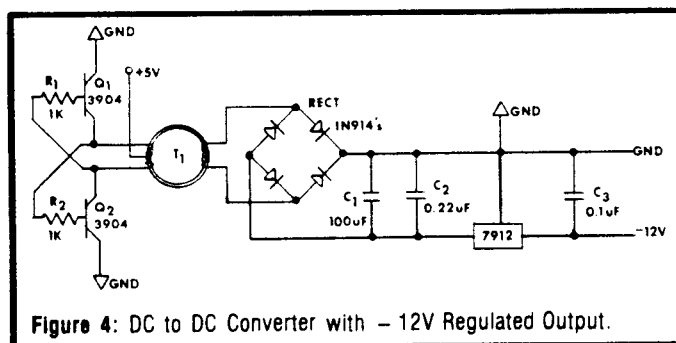


Figure 4: DC to DC Converter with -12V Regulated Output.

My favorite application for the DC to DC converter circuit is shown in Figure 5. This circuit configuration generates the plus and minus voltages required for an RS 232 serial interface. As you can see, the secondary is center tapped. With the center tap grounded, a negative voltage is obtained from one leg of the bridge rectifier and a positive voltage is obtained from the other. The RS 232 voltage

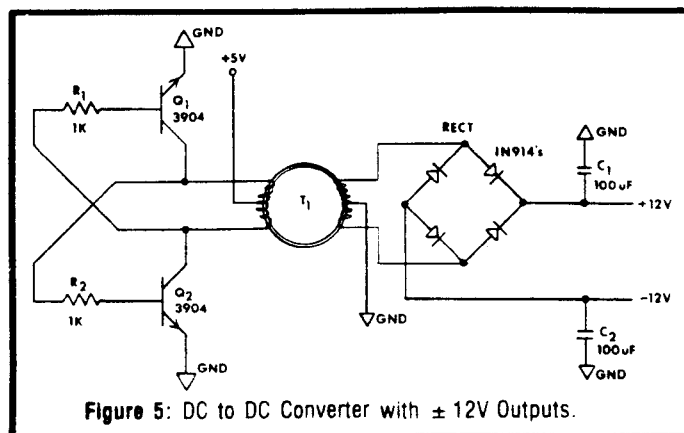


Figure 5: DC to DC Converter with ± 12V Outputs.

continued on page 22

# Multi-user

A Column by E.G. Brooner

While talking about networks and other multi-user systems, we should keep in mind that most of the concepts originated with large mainframe or minicomputer companies, and are just now being adapted to micros. This is for the same reason that micros themselves are popular, namely that they are more cost effective in the instances where they are adequate—as they indeed are for a great many applications.

As one of the pioneer microcomputer makers, Cromemco is in a position to take advantage of the current multi-user boom—they have done this with C-NET. C-NET is a true network, and exhibits most of the finer features that distinguish such systems from lesser lookalikes.

This system features a relatively high-speed data rate of 0.5 megabytes per second, true collision detection, and packet message construction. It uses the "bus" topology (in which all stations are effectively in parallel across a common transmission medium) and permits up to 255 users to be connected at any one time. It generally follows the OSI 7-level protocol system; the three lower, or network levels are hardware on a plug-in S-100 board and the transport (routing, etc.) is handled by associated software. Levels five, six, and seven of the OSI model are necessarily machine-dependent in any network operation and are not considered a function of the network itself.

Figure 1 is a photo (courtesy Cromemco) of their plug-in network board, which is most of what you need to adapt a Cromemco computer for network use. This is a standard S-100 (IEEE-696) board and although it was designed with their computers in mind, there is no fundamental reason it could not be used in any other S-100 bus computer. Figure 2 is Cromemco's illustration of a typical C-NET configuration.

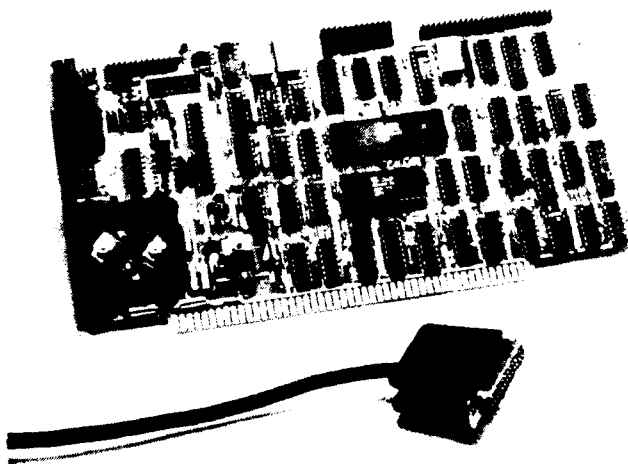


Figure 1

The functions they depict here are perhaps atypical of the installation that would be made by most small users; one of the interesting features they show is a *gateway* to a distant point. We have not previously discussed gateways in this column.

Earlier discussions described LANs as being very local in nature and confined, generally, to a building or relatively small complex. These limitations are imposed by the high speed at which networks usually operate. Long-distance communication is inherently at a slower rate. A gateway is a means of connecting a network, or some of its users, to a distant point. It may also connect two similar networks which, for some reason, cannot be totally combined. Communication with the distant point does not take place at high network speeds. The medium associated with a gateway may be telephone, satellite, or any other means of connecting two digital devices. Essentially, the gateway is an external connection, at which translations of speed and/or protocol may have to take place.

To understand gateways, we will have to discuss network protocols in a little more detail than we have in previous columns.

The International Standards Organization (ISO) has developed a plan known as the OSI, or Open Systems Interconnection model. This plan attempts to define all interactions between digital equipment, and between equipment and applications, as seven families of standards and protocols. The term "7-level protocols" is often used to describe this scheme. The RS-232 standard, the Centronics parallel standard, and the IEEE-488 bus are all level one protocols when viewed in this context—in other words, they are means of connecting equipment at the lowest level.

All methods of formatting data for transmission, such as SDLC, HDLC, and the various "packet" configurations, are level two protocols. It is important to note that the OSI model does not attempt to standardize any single protocol at any level, but only defines the functions that will be performed.

Needless to say, manufacturers do not always (as yet) follow this scheme. Ethernet, as an example, lumps levels one and two together and calls it "Ethernet;" this poses no problems unless one would try to interface something into an Ethernet between levels one and two. IBM and other mainframe makers usually have some kind of "network architecture" (such as IBM's SNA) that combine all of the low-level protocols in an inseparable manner.

Using the OSI concept, each level provides a transition to the next higher and next lower layers. It is apparent that if one network uses a certain type of level three or network control protocol, and another uses a different protocol for

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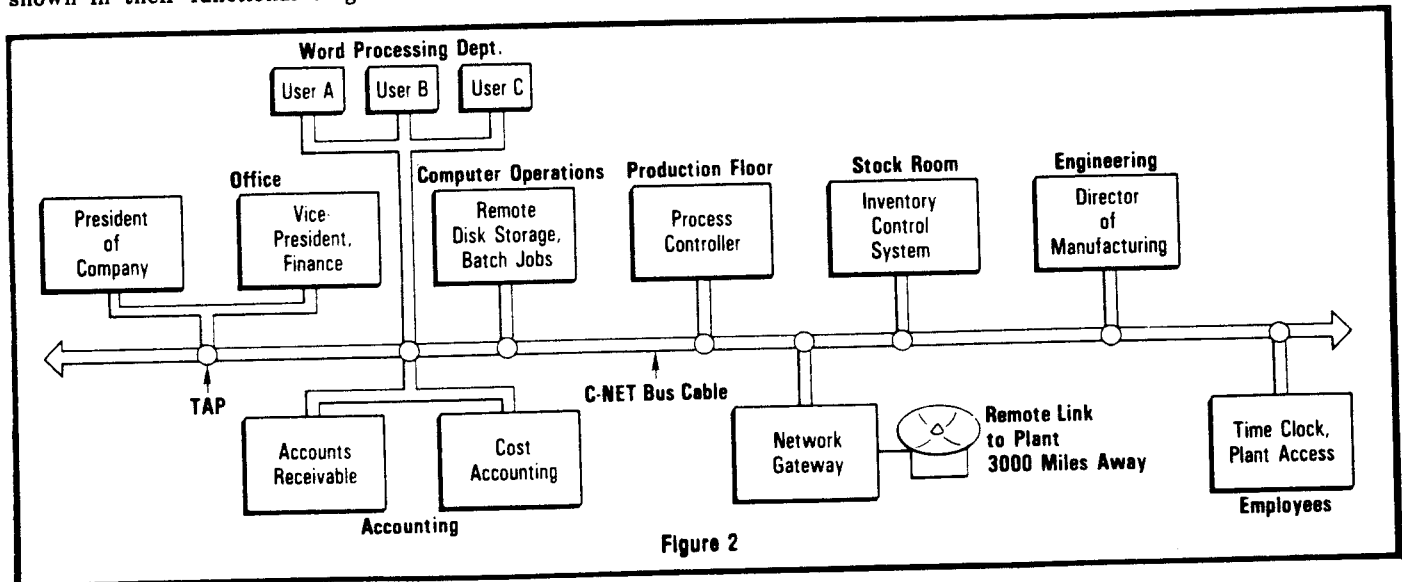
the same purpose, they are not compatible.

Finally, we get back to the concept of a "gateway." If at any point in a communication system it is necessary to translate from one protocol to another, at an equal level, a gateway is necessary. The gateway might change a format, a code, the speed of transmission, or the type of medium that is being used.

Cromemco does not advertise the details of the gateway shown in their functional diagram and, in fact, they may

have several different configurations for different purposes.

Now that we are on the subject of the protocol model, we should go ahead and define the rest of them as well as the state of the art permits. As explained earlier, level one is the direct connection of equipment, level two is the format of the transmission, and level three is the network control. There is no general agreement on the distinction between three and four—both are concerned with "transporting" data between points after it is *continued on page 22*





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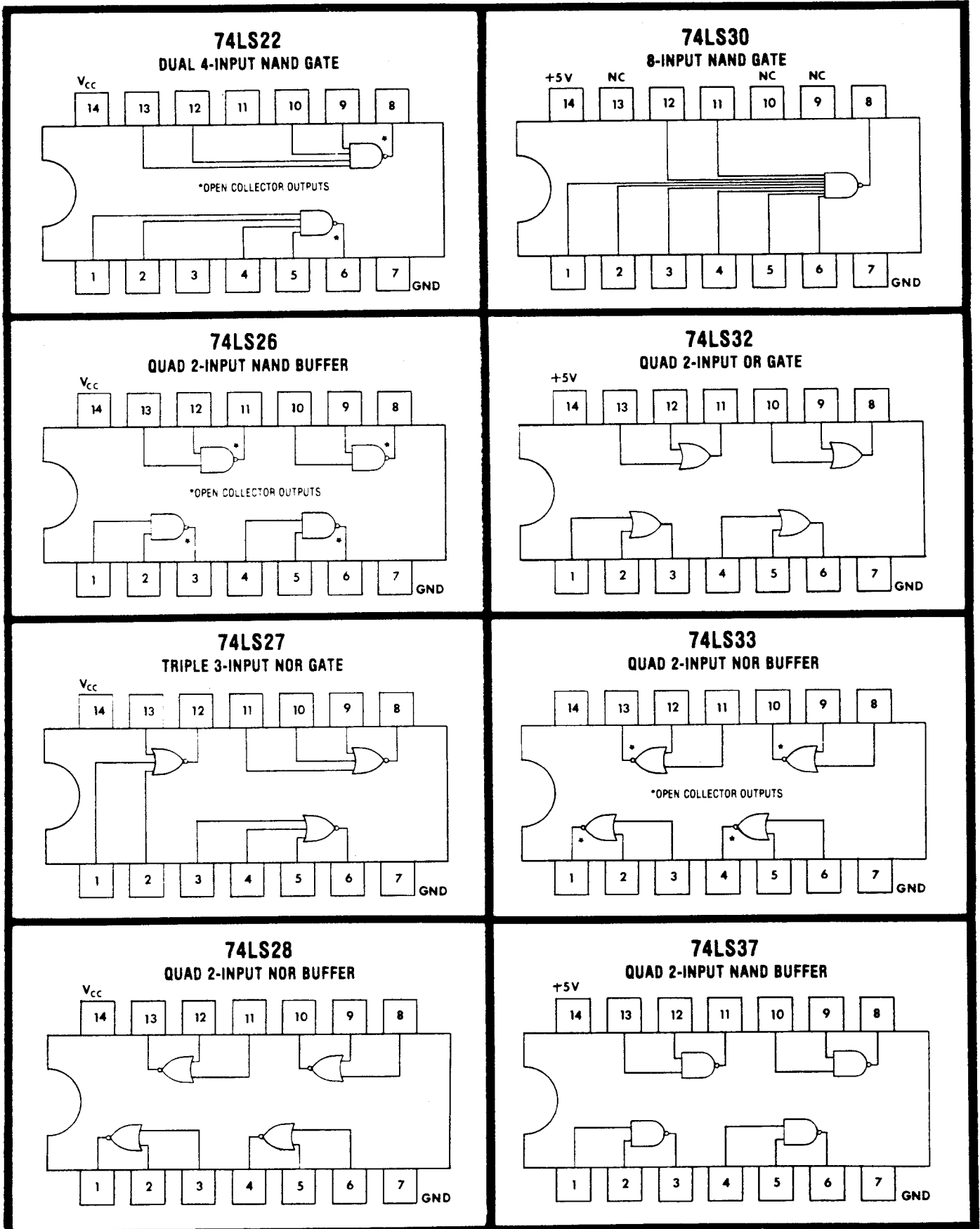
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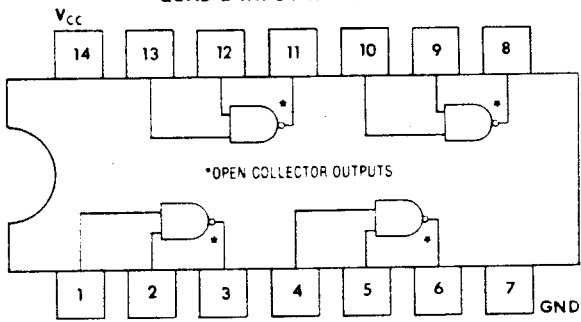
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# LSTTL Reference Chart



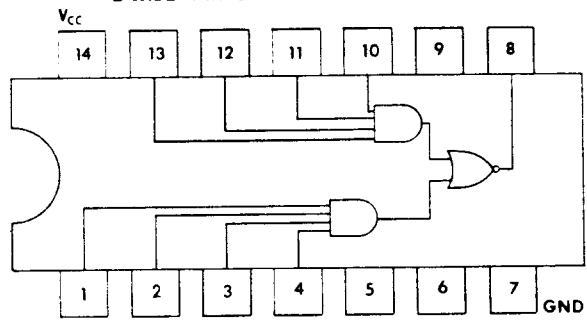
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**QUAD 2-INPUT NAND BUFFER**



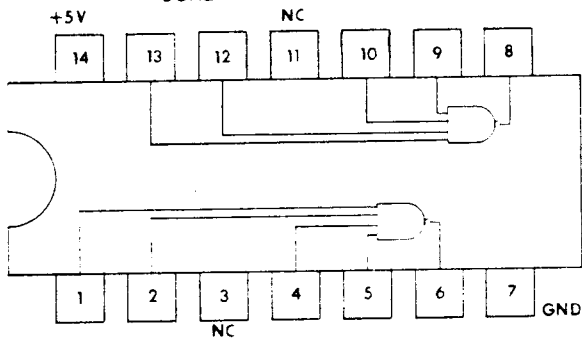
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**2-WIDE 4-INPUT AND-OR-INVERT GATE**



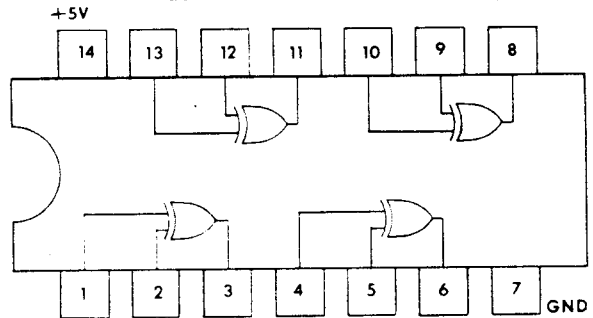
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**DUAL 4-INPUT NAND BUFFER**



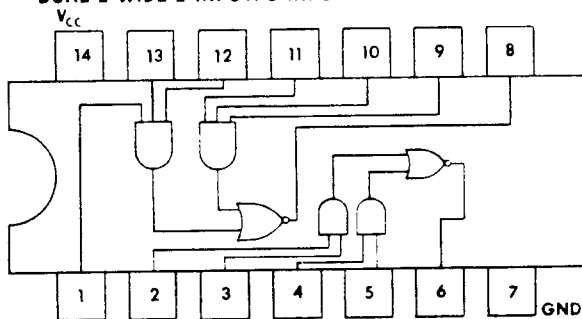
**74LS86**

**QUAD EXCLUSIVE-OR GATE**



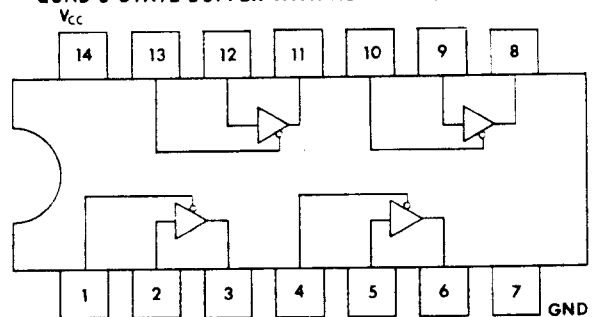
**74LS51**

**DUAL 2-WIDE 2-INPUT/3-INPUT AND-OR-INVERT GATE**



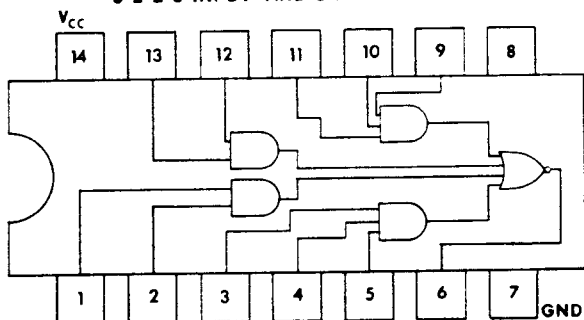
**74LS125**

**QUAD 3-STATE BUFFER WITH ACTIVE HIGH ENABLES**



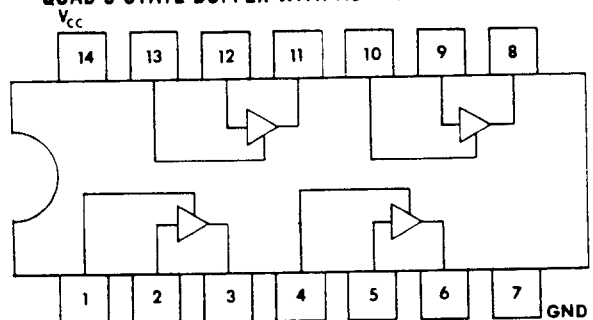
**74LS54**

**3-2-2-3-INPUT AND-OR-INVERT GATE**



**74LS126**

**QUAD 3-STATE BUFFER WITH ACTIVE HIGH ENABLES**



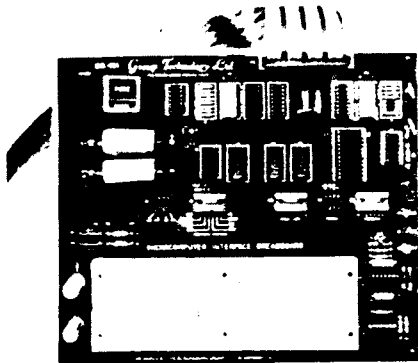
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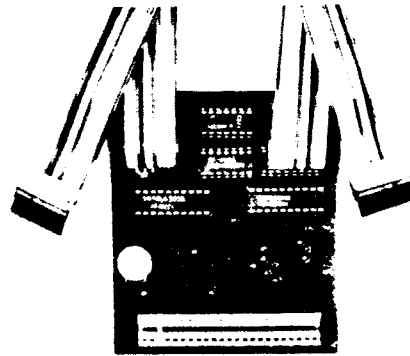
Versatile breadboards and clearly written texts with detailed experiments provide basic instruction in interfacing microcomputers to external devices for control and information exchange. They can be used to provide vivid illustrations of science principles or to design interface circuits for specific applications. Fully buffered address, data, and control buses assure safe access to decoded addresses. Signals brought out to the breadboards let you see how microcomputer signals flow and how they can be used under BASIC program control to accomplish many useful tasks.

Texts for these breadboards have been written by experienced scientists and instructors well-versed in conveying ideas clearly and simply. They proceed step-by-step from initial concepts to advanced constructions and are equally useful for classroom or individual instruction. No previous knowledge of electronics is assumed, but the ability to program in BASIC is important.

The breadboards are available as kits or assembled. Experiment component packages include most of the parts needed to do the experiments in the books. Connecting cables and other accessory and design aids available make for additional convenience in applying the boards for classroom and circuit design objectives. Breadboard prices range from \$34.95 to \$350.00



The INNOVATOR® BG-Boards designed by the producers of the highly acclaimed Blackburn Series of books have gained wide acceptance for teaching microcomputer interfacing as well as for industrial and personal applications. Detailed, step-by-step instructions guide the user from the construction of device address decoders and input/output ports to the generation of voltage and current signals for controlling servo motors and driving high-current, high-voltage loads. BG-Boards are available for the Apple II, II+, IIe; Commodore 64 and VIC-20; TRS-80 Model 1 with Level II BASIC and at least 4K read/write memory, Models III and 4. The books, *Apple Interfacing* (No. 21862) and *TRS-80 Interfacing Books 1 and 2* (21633, 21739) are available separately.



The FD-ZX1 I/O board provides access to the Timex-Sinclair microcomputer for use in automated measurement, data acquisition, and instrument control applications. A number of science experiments have been developed to aid teachers in illustrating scientific principles. The operating manual contains instructions for constructing input and output ports. A complete text of the experiments will be available later in 1984. The FD-ZX1 can be used with Models 1000, 1500, 2068, ZX81, and Spectrum.

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# DOS WARS

by Bill Kibler

In the three-part series on integrating systems (Vol. II, nos. 2,3, and 4), I discussed operating systems in general. Recently I was involved in a discussion at my computer club about the different types of operating systems and their merits. Many users, I am sure, still have some questions about which operating systems to use and why. It occurred to me that I should explain more about DOSs (disk operating systems) both for beginners and for those who work with them but sometimes forget what they're for. Understanding DOSs is becoming more important as a larger variety of systems is pushed by the manufacturers.

## DOS Designs

Digital Research Inc. made its name on the CP/M operating system. This system is the interface between the user and his computer. There are many different types of interfaces around. Some were even out before CP/M, but none provided such an open form of interface for independent writers of programs to use. Most interfaces before CP/M were company specific—that is, only software written by the company could run on their system. CP/M is an open standard which allows programs to move from system to system and is, for all practical purposes, independent of hardware considerations. This design opened up the microcomputer market and set the stage for the current DOS war.

CP/M was designed around the Intel 8080 device. This means that the machine code which comprises the program will run only on the 8080. The Zilog Z80 is a superset of the 8080 (contains the same machine instructions plus more special high speed functions) and will also run almost all CP/M programs unchanged. When used with an 8080 or Z80, CP/M is referred to as CP/M-80, as many newer versions of CP/M now exist. CP/M-86 is for the Intel 8086088, CP/M-88K for the Motorola 68000, CP/M-8K for Zilog's Z8000, and soon CP/M-16K for National's 16000 series of CPUs. All of these CPUs (central processing units) have 16 bit accumulators, whereas the 8080/Z80's is 8 bits. The other CPU enhancements concern the number of internal registers (temporary storage and pointers), the number of bits in each register, special register functions (indirect memory addressing), and how many address lines each can manipulate. Computers using the 16 bit CPUs can use more memory, perform larger calculations, and are supposed to be faster.

Before IBM, microcomputers were considered by many to be just hobby items. Although a lot of people were doing very meaningful things with their computers, if IBM didn't

do it, large business considered it a toy. When IBM entered the market, micros stopped being toys and many people bought their first computer (made by IBM). Due to financial considerations, IBM chose their operating system based on Microsoft's MSDOS. This program was originally written by Seattle Computers, and was adapted by Microsoft for the 8086088 system. It has the same open interface (CP/M-like) that allows programs to run independently of hardware. With IBM behind the system, MSDOS is now becoming the 16 bit standard, like it or not.

## The War Starts

As one can probably guess, war between lovers of CP/M and MSDOS has been raging in many publications. The companies have countered with updated versions and even newer systems (concurrent CP/M). AT&T recently jumped into the fray with their UNIX operating system (originally for CPUs with a 32 bit design) and many 16 bit versions of it. The hour-long discussion at my computer club was on which one of these systems is best, and which one should be bought and learned. The general feeling was that none of the new systems merit buying now, but that they should be watched closely. This position is based on the current capabilities and prices of these products.

In my articles on system integration I tried to stress the need for defining clearly in your mind why you are getting a computer. The same is true when dealing with operating systems. Choosing the wrong system will limit the number of off-the-shelf programs you can run. I use mostly public domain software and pay about \$5.00 per 8" disk of programs. However, if I didn't use a CP/M system many of these programs would have cost me several hundred dollars per disk (my library has about 40 user group disks). There are currently several 16 bit programs in the normally 8 bit public domain, and separate MSDOS user groups are being formed (one group already has 135 IBM PCDOS disks). This wealth of programs has almost eliminated program availability as a deciding factor in purchasing systems.

In part three of *System Integration*, I tried to point out why I felt CP/M 3.0 was not necessarily a good buy. I still feel that users of a 2.2 system are better off installing a RAM DRIVE than upgrading to 3.0. This also holds for upgrading to MSDOS or CP/M-86 even if the hardware is cheap. My personal home computer is a new Heath Z-100, bought so that I would have access to all possible worlds (S-100 bus, CP/M-80, MSDOS, and CP/M-86). Since writing articles is 80% of its use, CP/M-80 gets used 80% of the time. This has also given me a chance to test system speeds, and again CP/M-80 wins.

## System Design

When the IBM PC first appeared in the trade journals, I studied the articles closely, and decided that it was a poorly designed machine. Since then, several articles have appeared showing how slow and cumbersome its design is. These facts have not stopped first time users from spending \$4000 on the name. I would guess that many users are unaware of the system's poor features. Dedicated 2.2 users who use IBM usually become frustrated with its slow speed, and return to their favorite system. Why? CP/M 2.2 is a straightforward design, the DOS is located at high memory, and programs run from low memory just above a fixed entry jump table (8080 interrupt vectors set this design condition). When writing programs, little variation occurs between different systems to cause problems, and a lot of reference material is present to answer questions at non-technical levels. With 3.0, things start to get complex. Despite the fact that the same interface to the user is maintained, the operating system is in several parts, and data is moved into unknown parts using unknown algorithms.

MSDOS starts right out differently, with the DOS in low memory and the user program area after the DOS. Large memory is now necessary, offsets are used to determine which bank of memory is active, and 64K is still the largest continuous segment of program space usable. What this means to the user is a more complex system to understand, forcing the user to purchase programs. True, more complex programs can be run, but writing your own programs in anything other than BASIC is almost impossible. This fact is borne out by the IBM user disks which contain about 60-70% BASIC programs (including the disk utilities).

Not only should an operating system let you use programs (and be able to modify or understand them easily) but it must allow you to back them up (make copies), check density, catalog them, sort files, and many other disk utility functions. This is really where the battle is being fought—over utility functions. CP/M 2.2 has several built-in functions, and the open design allows for many utilities to support non-resident functions. The full operating system usually resides in less than 16K and can be used with only 10K of utilities beyond the system tracks. Approximately 170K is the normal free space on an 8" disk after I load my word processor and support utilities (250K after formatting). CP/M 3.0 uses a 32K system file plus system tracks (banked system) and may require up to 20K of support utilities. The same word processor and support programs would leave approximately 120K of 250K free. My favorite RAM DRIVE program only requires 4K of disk space and improves the speed to more than that of CP/M 3.0.

When looking at speed, the 16 bit systems have a major drawback; they do 16 bit moves on an 8 bit wide system. IBM uses the Intel 8088, a 16 bit wide device that talks to the system 8 bits at a time. This equates to two accesses for each full accumulator function. Since most PC programs are only conversions of 8 bit programs, optimization to use the 8 bit word moves is not always implemented. This means that two read or write functions must happen to load the accumulator. In true 8 bit systems only one read is needed

for many of the same operations, or the 8 bit systems will do it in half the number of program steps. Consider again that text is in ASCII code (my 80% word processing) which is 7 bits. and if 16 bit words are moved around, that wastes time. The only true test of speed is to try the system, since design is not the only thing to consider when comparing CPU capability.

## Dos Usage

Having taken a diversion to discuss the different types of CPUs, let's get back to the main problem—that of which operating system to use. When 2.2 came out, most programmers were new at writing DOSs, and users helped upgrade the system as much as did the manufacturer. Things are different now. Competition is fierce, and professional programmers abound. Like some doctors, many programmers want all the work for themselves with as little intervention from the user as possible. TURBODOS<sup>®</sup>, a high speed version of CP/M 2.2 and MP/M, is a good example of some programmers' positions. The authors are not available, and hide out somewhere unknown to all but their agents. Very tight registration procedures are used (to prevent freebee systems), and little how-to information is given. Although this program works fine, I would rather use one of the look-alikes of CP/M that provides the source listing. Although I don't plan or recommend changes in DOSs for anyone but experts, my experience has shown that such lack of information will only cause problems in the long run.

In order to make comparisons, you, the user, need to define the system's use. Unix is a programmer's operating system, best suited to professional programmers who use the operating system more than they do canned programs. When I make changes in a BIOS, the steps go something like this: 1) make change in BIOS, 2) ASM BIOS, 3) find errors, 4) change errors, 5) run program and find errors, 6) go back to 1. Doing that 20 to 30 times in an afternoon can get pretty frustrating with slow, cumbersome systems. My Z-100 takes about a minute to boot, and if testing the system involves booting, that makes the loop about 10 to 15 minutes long. Small, short BIOSs that can be loaded quickly are great for developing new systems, as are programs that provide outer and inner rings for programs to run in. In the 32 bit versions, UNIX takes 250k of memory and several megabytes of disk space, which is definitely not a home system. Although this system provides a lot of tools (programs for special functions) for the programmer, and has those rings that help develop new programs more quickly, these functions are all at the operating system level. Once inside a running program, most of the extra bells and whistles are lost.

## Not Getting Lost

What I have been attempting to do in this article is to give enough background on operating systems to keep you, the user, from buying useless programs. Most of these programs are not useless in the right hands, but advertising agencies can make you believe a child could run their

program. For all those fathers who bought toys that said "any child can assemble this," only to find that the child would have to be a prodigy—have no fear; these same people are now selling computers! One of the reasons I am glad to be writing for *The Computer Journal* is its lack of irrelevant product reviews. The big, glossy computer magazines spend more time selling systems than supporting those products already sold and running. This is usually known as selling out to big business, which I believe they have done. There are some fairly honest reviews in these publications, but they are intended to sell. When it comes to computers (and life too), the biggest, newest, and most expensive are not always the best. There are several good 2.2 systems for about \$1500 that are better than the PC's which sell for \$3800. Nothing surpasses an educated buyer when it comes to operating systems, but education must be tempered with a good understanding of your own limits, desires, and needs.

### A Parting Word

This article was intended to arouse your curiosity, make you think about computing, help you start understanding DOSs, and show that the industry has a lot of room for improvement. Articles never appear as the writer had originally intended, nor as the reader would like them, but magazines are also forums for discussion and can start new and important changes when people take an active part. Remember, the first 8080 computer started as a how-to article... so start using your computer and write in with your discoveries and opinions. ■

#### Multi-user, continued

formatted and after the devices have been connected in some manner. Sometimes we see references to "3A" and "3B" for these purposes. Levels five, six, and seven exist only within the computer and involve the way data is represented and its application, hence they are not really part of a network or communication system as such.

In any multi-user system we will find level one protocols of some kind, usually level two, sometimes three, and perhaps four. We note in Cromemco's literature that they do consider all of these protocols as separate entities and that is good engineering practice where networks are concerned. ■

*Cromemco and C-NET are trademarks of Cromemco, Inc. For additional information contact their marketing division at 280 Bernardo Avenue, Mountain View, CA 94043.*

#### Interfacing Tips, continued

specifications require that a logic 0 be between a +3 volts and a +15 volts, and a logic 1 be between a -3 and a -15 volts. Since there is such an allowable variation in voltages for each logic level, there was no need for regulation in this circuit. For this circuit I adjusted the converter output to generate a +12 volts and a -12 volts for the two logic levels. I have driven cables up to 25 feet using this configuration without any errors on the serial interface. ■

### Threaded Language, continued

```

#CAD: A5 #0          LDA SL          ; unneeded values
#CAF: 69 #4          ADC #0#4
#CB1: 05 #0          STA SL
#CB3: 90 #2          BCC #0#2
#CB5: E6 #1          INC SH
#CB7: 4C #9 #B #2    JMP ACC->      ; and return the answer
*
** */MOD **
*
#CBA: 05 AA AF CD 6E #C
#CC0: A0 #2          LDY #0#2          ; get the first two
#CC2: B1 #0          LDA (S),Y      ; unsigned numbers
#CC4: 99 #C #0       STA ACC.AL-2,Y
#CC7: C0             INY
#CC8: C0 #6         DEY
#CCA: D0 F6         BNE LOOP1
#CCC: 20 #A #B      JSR 16*16*32 ; multiply them
#CCF: A0 #3         LDY #0#3          ; move C -> B
#CD1: B9 14 #0 #0   LDA ACC.C1L,Y
#CD4: 99 10 #0      STA ACC.B1L,Y
#CD7: B0            DEY
#CDB: 10 F7         BPL LOOP2
#CDA: C0            INY
#CDB: B1 #0         LDA (S), Y      ; get the third
#CDD: 05 #E         STA ACC.AL      ; unsigned number
#CDF: C0            INY
#CE0: B1 #0         LDA (S), Y
#CE2: 05 #F         STA ACC.AH
#CE4: 20 4B #B      JSR 32/16=16 ; divide by it
#CE7: 20 #9 #B      JSR DROP      ; and go to the
#CEA: 4C 2B #C      JMP MODISH    ; end of /MOD
*
** ' **
*
#CED: 01 A1 A0 A0 BA #C
#CF3: A0 #1         LDY #0#1          ; put the address
#CF5: B1 #0         LDA (S),Y      ; in SCR
#CF7: 05 19         STA SCR.H
#CF9: B0            DEY
#CFA: B1 #0         LDA (S),Y
#CFC: 05 18         STA SCR.L
#CFE: 20 #9 #B      JSR DROP
#D01: B1 #0         LDA (S),Y      ; and store the
#D03: 91 18         STA (SCR),Y    ; value in (SCR)
#D05: C0            INY
#D06: B1 #0         LDA (S),Y
#D08: 91 18         STA (SCR),Y
#D0A: 4C #9 #B      JMP DROP
*
** + ' **
*
#D0D: #2 AB A1 A0 ED #C
#D13: A0 #1         LDY #0#1          ; put the address
#D15: B1 #0         LDA (S),Y      ; in SCR
#D17: 05 19         STA SCR.H
#D19: B0            DEY
#D1A: B1 #0         LDA (S),Y
#D1C: 05 18         STA SCR.L
#D1E: 20 #9 #B      JSR DROP
#D21: 10            CLC
#D22: B1 #0         LDA (S),Y      ; and add the value
#D24: 71 18         ADC (SCR),Y    ; to (SCR)
#D26: 91 18         STA (SCR),Y
#D28: C0            INY
#D29: B1 #0         LDA (S),Y
#D2B: 71 18         ADC (SCR),Y
#D2D: 91 18         STA (SCR),Y
#D2F: 4C #9 #B      JMP DROP
*
** C ' **
*
#D32: #2 C3 A1 A0 #D #D
#D38: A0 #1         LDY #0#1          ; put the address
#D3A: B1 #0         LDA (S),Y      ; in SCR
#D3C: 05 19         STA SCR.H
#D3E: B0            DEY
#D3F: B1 #0         LDA (S),Y
#D41: 05 18         STA SCR.L
#D43: 20 #9 #B      JSR DROP
#D44: B1 #0         LDA (S),Y      ; and put the
#D46: 91 18         STA (SCR),Y    ; one-byte value
#D4A: 4C #9 #B      JMP DROP      ; in (SCR)
*
** # # **
*
#D4D: #1 C0 A0 A0 32 #D
#D53: A0 #1         LDY #0#1          ; put the address
#D55: B1 #0         LDA (S),Y      ; in SCR
#D57: 05 19         STA SCR.H
#D59: B0            DEY
#D5A: B1 #0         LDA (S),Y
#D5C: 05 18         STA SCR.L
#D5E: B1 18         LDA (SCR),Y    ; and get the value
#D60: 91 #0         STA (S),Y      ; from (SCR)
#D62: C0            INY
#D63: B1 18         LDA (SCR),Y
#D65: 91 #0         STA (S),Y
#D67: 60            RTS
*
** # # **
*
#D68: #2 C3 C0 A0 4D #D
#D6E: A0 #1         LDY #0#1          ; put the address
#D70: B1 #0         LDA (S),Y      ; in SCR
#D72: 05 19         STA SCR.H
#D74: B0            DEY
#D75: B1 #0         LDA (S),Y
#D77: 05 18         STA SCR.L
#D79: B1 18         LDA (SCR),Y    ; and get the
#D7B: 91 #0         STA (S),Y      ; one-byte value
#D7D: 90            TYA
#D7E: C0            INY
#D7F: 91 #0         STA (S),Y
#D81: 60            RTS

```

In conclusion, I hope you find this DC to DC converter circuit useful. I am interested in hearing about any unique applications that you might develop for it. Drop us a line and let us hear your ideas. ■

# BUILDING A CODE PHOTOREADER

by R.O. Whitaker

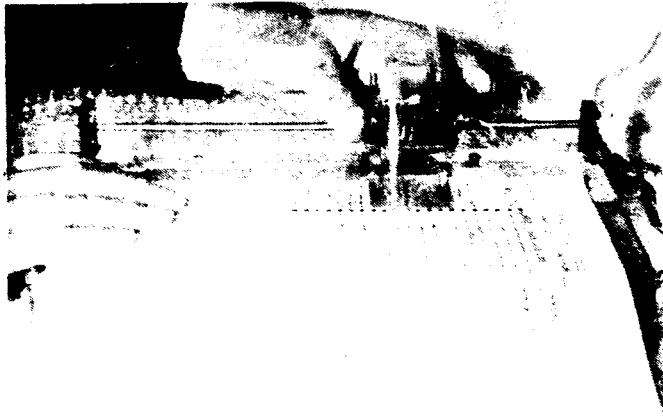


Figure 1: Reading the code into the computer.

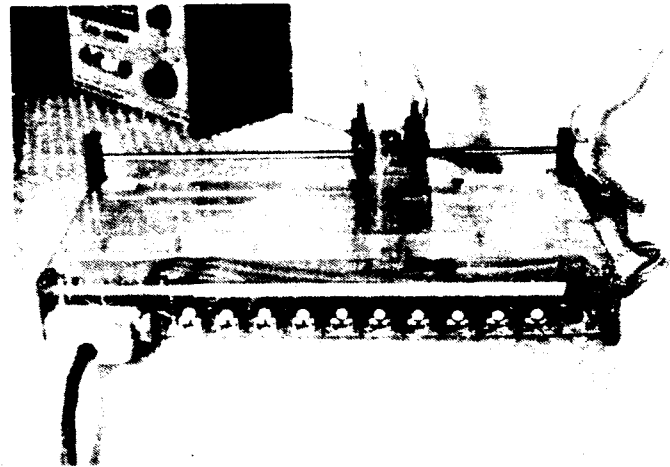


Figure 2: The reader. Electronics mounted beneath forward edge of platen. Seven zeroing pots shown in photo.

## Introduction

I don't key programs into my computer any more. Instead, I put the code sheets in my photoreader, pull the scanner down the code column, and in goes the code. But it is really not all that easy, because the code has to be written in "Computer Compatible Digits" (CCD). First, I had to learn to read and write them. What is a "Computer Compatible Digit?" Look at Figure 3. The elements of the code are binary weighted. Since each element corresponds to a respective bit of a computer word, the digit is "Computer Compatible," and no encoding is required for going to or coming from the computer. The digit is inherently hexadecimal, as indicated at the bottom of Figure 3.

The first CCD was proposed by a gentleman over in Prague about 1955. Since then, several others have proposed digits of various configurations. The one I use was discussed in a paper published in an electronics magazine several years ago. All of the digits except six and seven can be written without lifting the pencil from the paper. All elements are equally conspicuous, and the elements of each

digit are mutually contiguous.

Figure 4 is a coding sheet with the code column on the left. The CCDs are formed by connecting the appropriate dots with a dull #2 pencil.

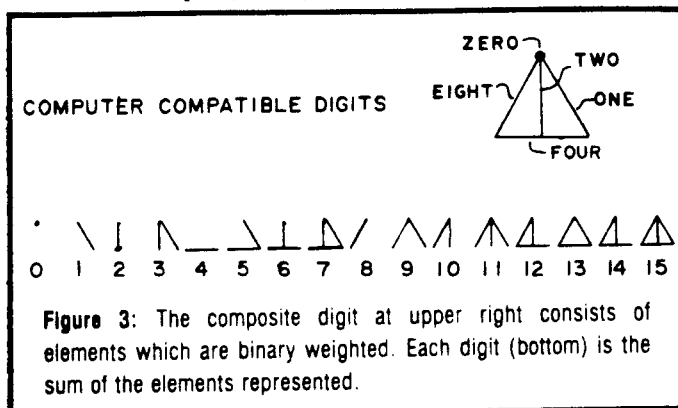
Figure 5 shows the basic structure of the photoreader with a Code Sheet on the platen. The left edge of the sheet is placed against the stop to assure proper horizontal registry. The scanner slides on the guide rod. The optical fibers pass through holes in the faceplate (which slides over the code column).

The scanner has a carrier associated with it which moves under the platen and keeps a pair of pilot lamps opposite the fiber ends. Light shines up through the transparent plastic platen and through the paper. Consequently, each fiber receives light except when it passes over a line of one of the digits. The other ends of the fibers feed to a series of photodetectors which are mounted on top of the scanner. The signals are then led by the ribbon cable to the electronics mounted under the forward edge of the platen (see Figure 2).

To operate the photoreader, insert the code sheet and move the scanner to the top of the column. Lift sense switch 80 on the computer. Draw the scanner down the page. Drop SSW 80, remove the code sheet, and insert the next one.

The fiber optic sensors scan along the dotted lines of Figure 6. Note that the ID (indicium) sensor senses the presence of indicia in the column at the right. The action is as follows:

1. When the ID sensor leaves an indicium, it causes the "B" register of the computer to be nulled. The word being scanned will be assembled in this register.
2. While the ID sensor is in the "A" region of Figure 6, the other six sensors look for their respective lines. Each one





that sees its line sets its respective bit in register B.  
 3. While the ID sensor is in region B, the 8-sensor looks for the 4-line. If it sees the 4-line, it sets the 4-bit in register B. Similarly, the 80-sensor looks for the 40-line and sets the 40-bit.

4. When the ID sensor drops from the indicium of region B, the word in register B is delivered to memory and to the display. Register B is reset before scanning the next word.  
 The "2-lines" were not included in Figure 6, but appear in

Figure 4. Note that each 2-line bears a crossbar, which causes the 2-sensor to see the line even if the paper is off a millimeter or so in horizontal registry or if I was too sloppy in writing it.

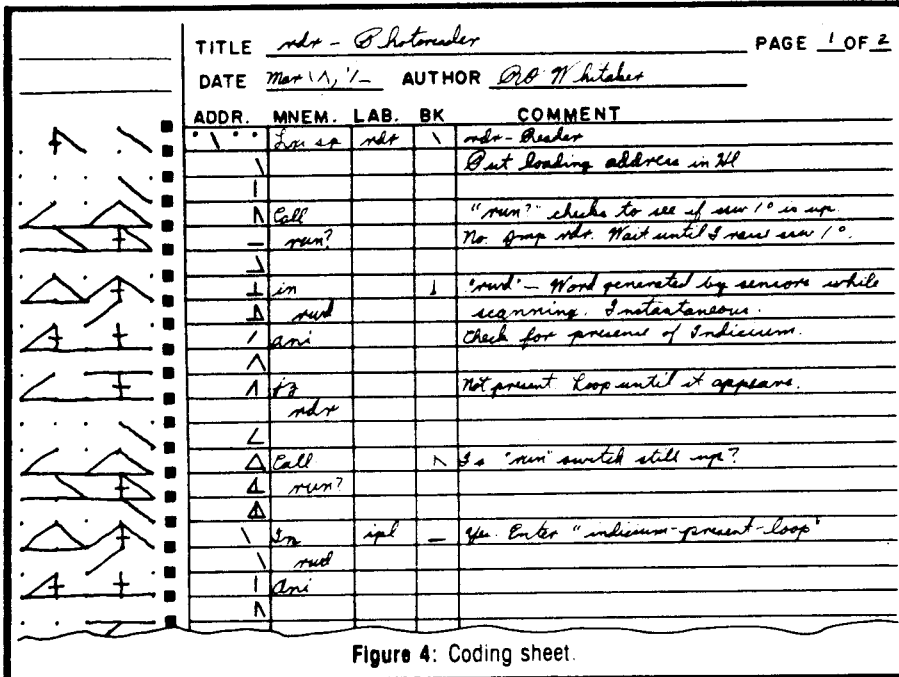


Figure 4: Coding sheet.

**The Flowchart**

Refer to the flowchart in Figure 7. Blocks one to four initialize the system. Blocks five to end constitute the RUN loop in which the computer operates while characters are being read. Blocks six to nine constitute the A loop, where the computer operates as long as the ID sensor is in region A. Blocks ten to thirteen are the B loop where the computer operates while the ID sensor is in the B region. Blocks fourteen to end terminate the reading of a pair of digits.

The blocks will now be discussed in order.

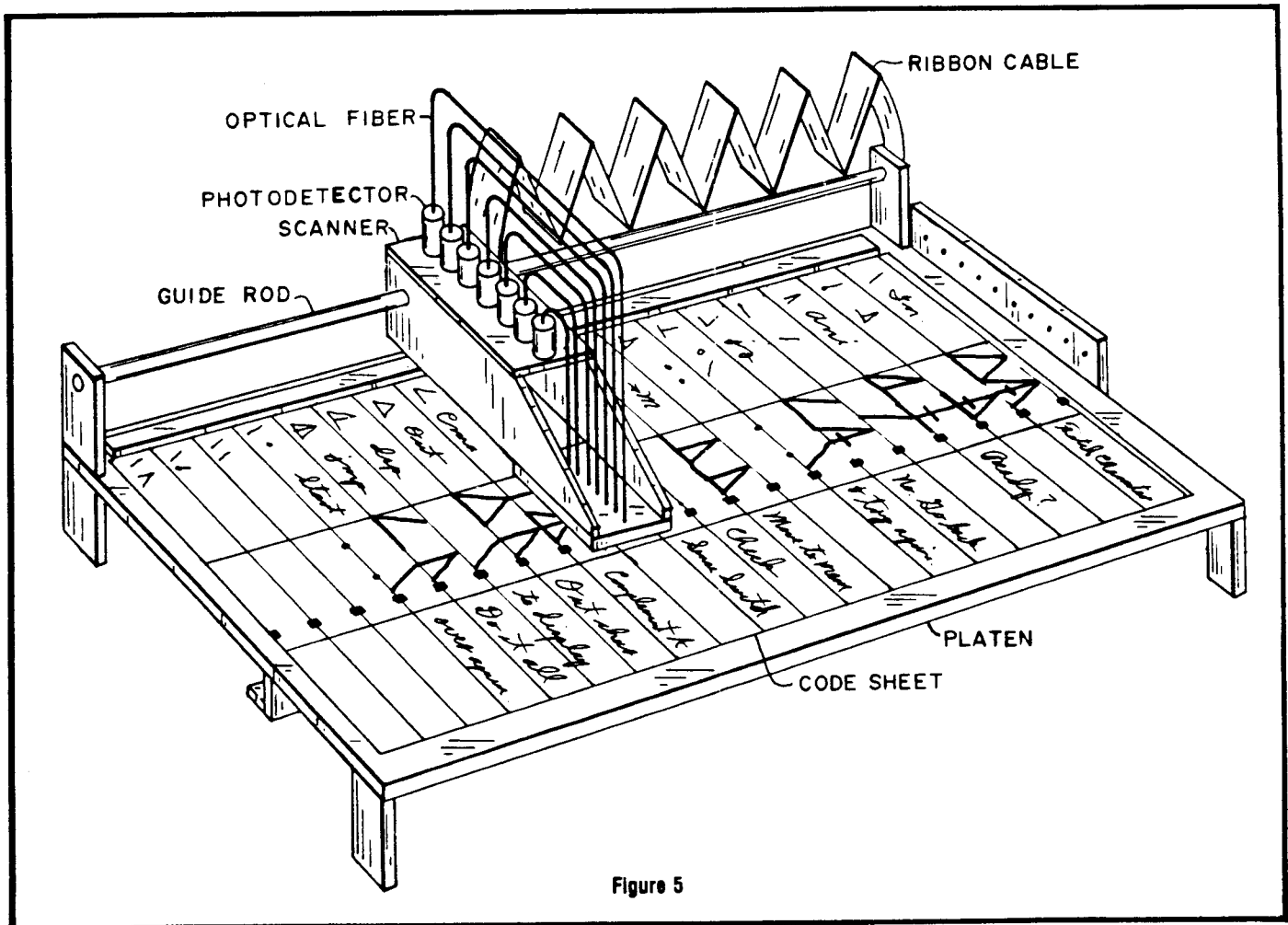
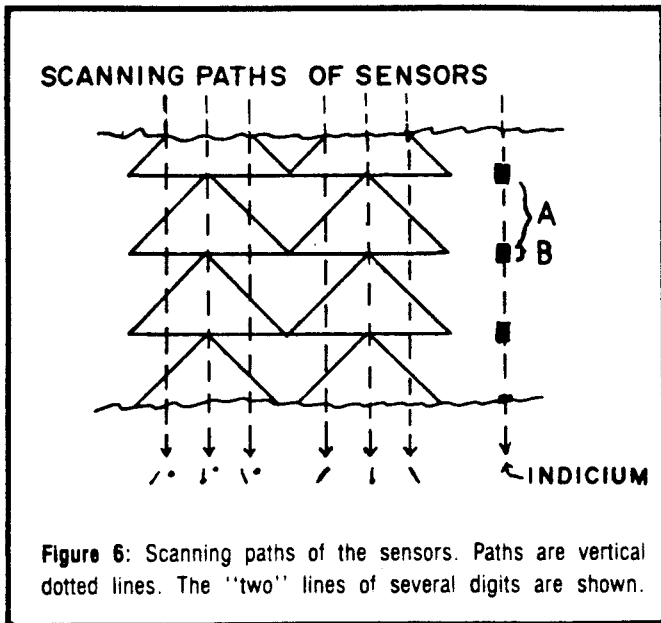


Figure 5



1. The computer twiddles until SSW 80 is lifted. This prevents anything from being read until I have zeroed the pots, given the computer a loading address, have the code sheet in place, and am ready to read.
2. As soon as SSW 80 is raised, the computer drops to here. If the first indicium is not yet seen by the ID sensor, the computer continues to twiddle.
3. As soon as the top indicium (see Figure 3) is sensed by the ID sensor, the computer drops to here. If the first indicium is not yet seen by the ID sensor, the computer continues to twiddle.
4. If SSW 80 is still up, the computer drops to here. It checks to see if the indicium is still visible. Yes. It twiddles in a new loop.
5. As soon as the ID sensor drops off the top indicium, the computer drops to here. This block nulls the B register before the word being read is assembled into that register. The "PWD" stands for "Processor Word." The word is assembled in register B and moved to memory.
6. Checks to see if SSW 80 is still up. No. It aborts the scan.
- 7, 8, and 9. Checks to see if the SSW 80 is still up. Yes. Brings in the "Read Word" (RWD) sensed by the reader at any particular instant and dependent upon where the scanner happens to be in relation to the digit pair. Merges it into B. Repeats Steps six through nine until the ID sensor senses the presence of the second indicium. Note from Figure 6 that this loop will operate for region A. It will cause the 1, 2, 8, 10, 20, and 80 lines to be read. For each line present, it will cause its respective bit in register B to be set. Note from Figure 6 that a 1 or 8 line can hardly be mistaken for a 2-line.
10. Once the ID sensor sees the second indicium, the computer drops to here.
- 11, 12, and 13. This is the B loop. The computer stays here as long as the ID sensor sees the second indicium—as long as the sensors are in region B of Figure 6. The 80 and 8 sensors look for the 40-line and the 4-line respectively. The other sensors do nothing. If the 80-sensor sees the 40-line,

the 40-bit is set in register B. If the 8-sensor sees a 4-line, the 4-bit is set.  
 14, 15, and last. When ID drops off the second indicium, the word stored in register B is sent to memory and to the display. The memory pointer is incremented.

At the completion of scanning, I drop SSW 80 to prevent any more reading. A copy of the program (written for an 8080 computer) will be forwarded upon request. Send three 20 cent stamps to the author.

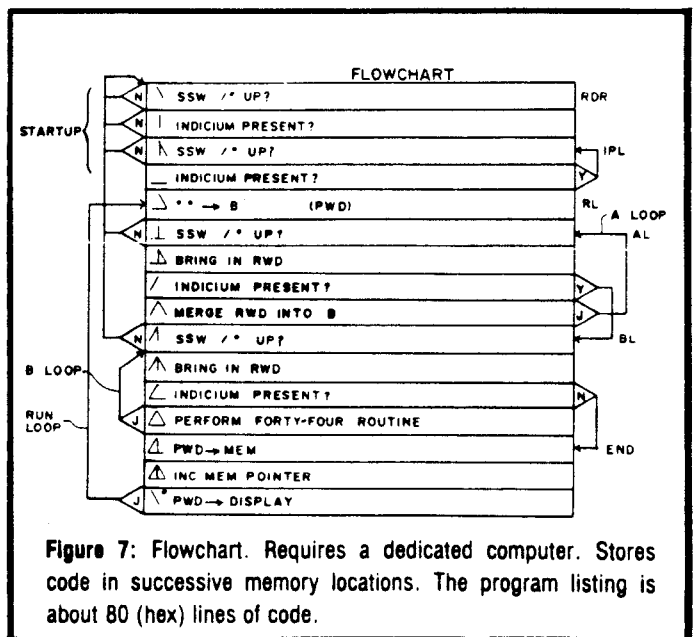
### Electronics

Study Figure 8 for a moment. The transistors and associated components were mounted on a piece of perfboard under the platen, as shown in Figure 2. Pots were mounted so that they could be easily adjusted from the front. The LEDs were placed beside their respective pots. Since there is no 4-sensor, the ID sensor occupies the 4 slot.

The Schmitt trigger (7413) was installed on the output of the ID sensor to eliminate multiple readings associated with noise signals when the sensor moved over the edge of an indicium. The pots permit the channels to be "zeroed." G.E. specifies three volts for proper operation of the photodarlington. Zener Z-1 drops the five volt supply to this level.

### Construction

I used scrap plastic obtained from a local plastics dealer for the frame parts and the platen. It seems that plastic is transparent to infrared radiation of the wavelength to which the sensors are sensitive. Hot glue was used to hold minor components in place. The guide rod on which the scanner slides was an iron rod taken from an old Selectric typewriter. It was already ground smooth, permitting the scanner to slide easily upon it. Any smooth steel rod about 4mm in diameter should do. Plastic Crofon optical fibers 1mm in diameter were used. The General Electric GFOD-1B photodarlington was designed to work with these fibers.



The open ends were polished with jeweler's rouge, and fit flush with the bottom surface of the faceplate. A piece of Scotch tape protected the exposed ends from abrasion. The holes for the fibers were drilled with a Unimat lathe, which permitted them to be positioned very precisely. However, that should not be necessary. If the digits are about 1.5cm in width, then a scale and centerpunch should allow the holes to be positioned with sufficient accuracy.

I used two six volt, 200ma pilot lamps for the light source, and surrounded them with a reflector made from a beer can. The two bulbs are powered by five volts regulated. I used a five volt bench supply to power the reader. Power could also be drawn from the host computer, or a supply could be mounted on the reader.

### Zeroing the System

To aid in zeroing the system, I put two horizontal lines across the top of the code column (see Figure 4). The first is so thin that the sensors do not trip on it. The second is just barely dark enough to trip the sensors. The pots were then adjusted so that their respective LEDs did not light for the first line and did light for the second. The only requirement for proper reading is that the lines of each digit be darker than the second line.

### Paper

At first I used a pad of dime store paper that was cross-hatched into 5mm squares. Any paper used should be free of clay—clay is opaque to infrared. I now use preprinted forms. They are more expensive and don't work a bit better, but they do make a more favorable impression upon the impressionable. Dots on the form are positioned so that the procedure of writing the code is reduced to connecting the appropriate dots with fairly straight lines.

### Future Models

Small diameter sensors are now available which can be mounted in the read head, eliminating the optical fibers. Should I build another reader, I will go that route. It would probably be better to replace the lamps with infrared emitters of the semiconductor type designed to work with the detectors. The two ordinary bulbs I used worked fine, but ideally, an emitter with a lens would focus radiation upon the paper directly opposite its respective sensor.

### Where to Get the Parts

The detectors should be procurable from your local GE distributor. The transistors and Schmitt triggers can be purchased from any Radio Shack or electronic parts store, or from a mail order company such as Jameco. I got my

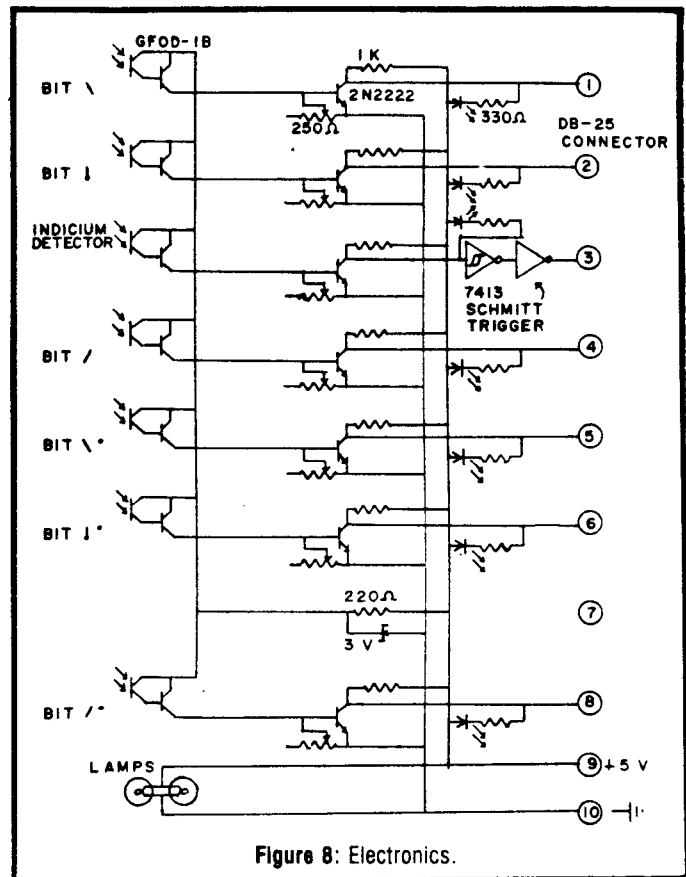


Figure 8: Electronics.

Crofon optical fibers from Edmund Scientific. Crofon is made by DuPont, and you can probably obtain it from a local plastics distributor. Check with GE. The matching connectors for the GFOD-1B were the most difficult parts to obtain. My source made me buy far more than I needed, and at an astronomical price. Check with your GE distributor regarding matching connectors, or check with me. If there is enough interest, I'll stock parts for resale at a nominal price. Hot glue or cement are viable alternatives to the connectors, but are not as fancy looking. The connectors are also considerably more convenient if you have to take the rig apart.

I have applied for a patent on the reader, and will sell you a non-exclusive license to build one unit for your own use. The cost to you will be one stamped, self-addressed envelope. The stamp should be of the 20 cent variety. And uncanceled. If you don't have one, let it go. Maybe I can find one around here. ■

R.O. Whitaker  
4719 Squire Drive  
Indianapolis, IN 46241

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Dear Computer Journal,

I need information on interfacing a TI 99YA with a Teletype model 28.

Wilbur Kespert  
Florida

*Ed: Readers, can you help?*

Dear Computer Journal,

Do you know how I could upgrade a TRS-80 MC-10 micro color computer to 64K using 4164 chips? Radio Shack makes a 16K plug-in module, but no 64K module.

Bryan Lepkowski  
New York

*Ed: Readers, can you help?*

Dear Mr. Rose,

I have read your three part article on building a print spooler with great interest. I am seriously considering the project. I do have one question. I have an Apple II+ and

some experience programming the 2716. I would like to know how I can handle the Z80 op codes with my "Big Mac" assembler. Could I enter the machine code directly into memory and then into the 2716? If so, could you provide me (and perhaps other readers) with a memory dump for the operating program?

Thanks,  
Hugh McEntire  
California

*Ed: Although I don't have an Apple II+ myself, I asked someone local here about the "Big Mac" assembler and he informs me that it can only handle the 6502 op codes and will not assemble those for the Z80. However, the program is not a long one, and your idea of entering it directly in machine language should be quite feasible. I made a hex dump of the operating program and am including it for you here.*

*Thanks for writing and good luck with your project.*

Regards,  
Lance Rose  
Technical Editor

```

0000 01 00 00 11 00 08 21 00 08 78 B1 CA 29 00 DB 01
0010 E6 01 CA 29 00 DB 01 E6 80 CA 29 00 1A D3 00 0B
0020 13 7A FE 80 C2 29 00 16 08 DB 01 E6 02 CA 09 00
0030 DB 00 77 03 23 7C FE 80 C2 3D 00 26 08 78 FE 77
0040 C2 09 00 79 FE F0 C2 09 00 3E 00 D3 01 DB 01 E6
0050 01 CA 75 00 DB 01 E6 80 CA 75 00 1A D3 00 0B 13
0060 7A FE 80 C2 68 00 16 08 79 FE E0 C2 75 00 3E 02
0070 D3 01 C3 09 00 DB 01 E6 02 CA 4D 00 79 FE FF CA
0080 92 00 DB 00 77 03 23 7C FE 80 C2 4D 00 26 08 C3
0090 4D 00 76

```

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# Books of Interest

## Interfacing Microcomputers to the Real World.

by Murray Sargent III and Richard L. Shoemaker.

Published by Addison-Wesley, Inc.

288 pages, 6¼ × 9¼, softbound, \$15.55.

This book covers interfacing using the Z80 microprocessor. It starts with the elementary principles of microelectronics and then uses them to explain more complex interfacing concepts. The examples are useful, practical applications including interrupts, real time clocks, stepper motors, A/D and D/A conversion, an interface board, transmitter and receiver circuits (garage door opener), and BSR carrier wave control circuits.

The contents are as follows:

•**Chapter 1 Introduction to Digital Logic.** The Diode, TTL Gates—AND, NAND, OR, NOR, XOR, The transistor as a Switch, TTL Input/Output Characteristics, Flip-flops, Clocks, Counters, and One shots and Shift Registers.

•**Chapter 2 Programming the Z80 Microprocessor.** Machine and Assembly Languages, Moving Data in 8-bit Registers and Memory, Manipulating Data—INC, SET, ADD, AND, 16-bit Registers and Memory Pointers, Jumps, Conditional Jumps and Subroutines, Shifty Registers, Input/Output, The Stack and A Tiny Operating System.

•**Chapter 3 Processor-Input/Output Interfacing.** The Forty Pins, Input/Output Ports, Input/Output Address Decoding, Interrupts, Real Time Clock Interrupt Scheme, Direct Memory Access (DMA), and I/O Example: Multiplexed Keypad/Display.

•**Chapter 4 Controlling/Monitoring Various Real World Devices.** Switch Closures, Input and Output, Digital to Analog Conversion, Analog to Digital Conversion, Signal Averaging and Lock-in Detection, Waveform Generation and Recognition, Motor Control, and Raster Displays.

•**Chapter 5 Serial Input/Output.** Parallel/Serial Conversion: the USART, RS232 and Current-loop Conventions, Modems, Computer-Computer Communication Methods, and Rf, Fiber Optics, and Power-line Carriers.

•**Chapter 6 Microcomputer Systems.** RAM, EPROM, Hard and Floppy Disks, Small Controller Systems, Z80 Computer Busses, and Examples of Larger Microcomputers.

•**Chapter 7 Software.** Editors, Assemblers, Linkers, Debuggers, Interpreters and Compilers, Disk Operating Systems, and Computer Hierarchies.

•**Chapter 8 Hands-On Experience.** TTL Logic, Assembly Language Programming, Building an Interface Board, Looking at CPU Signals, Interrupts and Real-time Clocks, Using I/O Ports as Device Controllers, Experiments with DACs and ADCs, Stepper Motors, and Serial and Computer-computer Communications.

•**Appendices** include the following: Z80 Buses—S-100 Bus Definition, TRS-80 Bus Definition, STD Bus Definition; Computer-Computer Communications—TRSCOM; The DEMON Monitor; Tiny Operating System; Keyboard/Display Routines; and Z80 Instruction Codes.

The entire book is very good, but I found the chapter on hands-on experience especially helpful. This chapter starts with two quotations, "Experiments should be reproducible; they should all fail in the same way," and "Experience is directly proportional to the amount of equipment ruined." These are attributed to Murphy, but anyone who has spent much time at the bench should agree. An example of the practical advice is found on page 190, where they say "Always wire up your circuits with the power OFF. When you are finished wiring, double check that the circuit is wired correctly BEFORE you turn the power on. The alternative is to check the circuit after the power is on and to observe which components have smoke rising from them."

This book is a good blend of theory and practical applications for anyone who wants to interface their Z80 microcomputer to the real world. ■

Art Carlson

### RPN (Reverse Polish Notation)

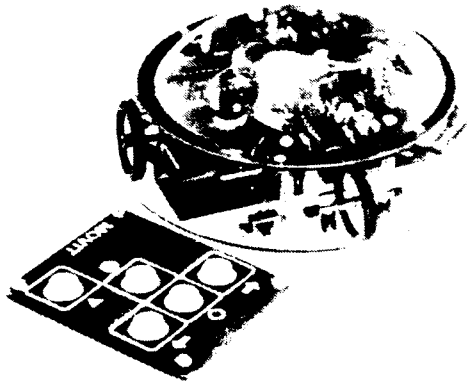
RPN (also known as postfix notation) is commonly used on stack oriented machines, and makes complicated algebraic expressions easier to enter. Using RPN, the operator is listed after the operands instead of between them. For example:

Std. notation	RPN
$3 \times 2$	3 2 ×
$4 + 5$	4 5 +
$7 / 3$	7 3 /
$2 + 4 / 3$	2 4 + 3 /

# New Products

## Programmable 4K RAM Robot

A new, low cost, programmable 4K RAM robot introduced by Stock Model Parts is controlled through its seven function teach pendant. The robot includes an on-board CMOS static RAM 256x4 sequencer. Applications include school science projects, robotics courses or personal enjoyment. Of special significance is the fact that the robot is programmable through any of the popular microcomputers (with parallel interface) to gain experience about how real robots are controlled. Buttons on the teach pendant can be used to program the robot to go forward, right, left, pause, sound a buzzer, light a LED lamp, or repeat a program continuously.



The three wheeled robot, called the Memcon Crawler, is offered in kit form. Included are four pages of easy to follow instructions which make it possible to complete the mechanical assembly in about two hours. All electronic elements are contained in two pre-soldered and pre-tested printed circuit boards. The 5½" diameter, 2½" high robot consists of 51 major components plus over 140 fasteners. Among the major parts are two DC motors, rugged blue tinted molded body parts, plus two geartrain assemblies. It is powered by one nine volt and two AA batteries.

The kit is available for \$79.97 postpaid from Stock Model Parts, Division of Designatronics, Inc., 54 South Denton Ave, New Hyde Park, New York 11040. ■

## MicroSolutions' New UniForm

MicroSolutions has developed a product called UniForm, which makes it possible to read and write 5¼" CP/M disks in a number of popular formats. UniForm is a program that allows the user to redefine the operating format of the "B" drive of their CP/M computer, opening up a whole new avenue of communication between systems with varying disk formats.

With UniForm, the user has the ability to take a blank

5¼" disk and initialize it to any of the supported formats. For example, you could initialize a disk on your KayPro II in the Morrow MD2 format, set your operating format to MD2, write a letter using WordStar, and mail it to someone with an MD2 who could use WordStar on their machine to read it. UniForm works with any files, text, data, or machine code. It does nothing to alter the files at all, and is transparent to the user or program while in operation. Programs with no video attribute or hardware dependent routines can be transferred between machines and run (such as PIP, or MBASIC programs if properly written).

UniForm is completely menu driven and self prompting, with English messages in response to invalid entries. The program was written with a heavy emphasis on ease of use, and as a result, is so straightforward that a manual is practically unnecessary. A manual is provided with UniForm. It explains the program simply and accurately, and provides a complete walk-through of all functions for those who desire it.

UniForm is able to support almost all 48 track per inch soft sectored CP/M formats. Since it is hardware dependent, versions are available for several of the most popular computers. Currently, there are eleven versions of UniForm: Actrix; Epson QX-10, KayPro II, 4, 4-84, and 10; Morrow Micro Decision; NEC PC-8801; Osborne I (DD); Televideo TS 803/TPC-1; and Zenith Z-100 CP/M-85. Some computers can support more formats than others because of internal hardware characteristics; for example, the Morrow MD UniForm supports 20 single sided formats, 18 double sided formats, and one non-CP/M format (the MSDOS/PCDOS). For a complete list of the formats available with any of these versions, write to MicroSolutions, 125 South Fourth St, DeKalb, IL 60115. UniForm is available from MicroSolutions for \$69.95. ■

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